

### XFP-10GB-DW44-100-PRO

MSA and TAA Compliant 10GBase-DWDM 100GHz XFP Transceiver (SMF, 1542.14nm, 100km, DOM, 0 to 70C, LC)

#### Features

- INF-8077i Compliance
- Temperature-stabilized EML transmitter and PIN receiver
- Duplex LC Connector
- Commercial Temperature 0 to 70 Celsius
- Single-mode Fiber
- Hot Pluggable
- Excellent ESD Protection
- Metal with Lower EMI
- RoHS Compliant and Lead Free



#### Applications:

- 10x Gigabit Ethernet over DWDM
- 8x/10x Fibre Channel
- Access, Metro and Enterprise

#### Product Description

This MSA Compliant XFP transceiver provides 10GBase-DWDM throughput up to 100km over single-mode fiber (SMF) using a wavelength of 1542.14nm via an LC connector. It is built to MSA standards and is uniquely serialized and data-traffic and application tested to ensure that they will integrate into your network seamlessly. Digital optical monitoring (DOM) support is also present to allow access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

Proline's transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S. – made or designated country end products.



## Regulatory Compliance

- ESD to the Electrical PINs: compatible with MIL-STD-883E Method 3015.4
- ESD to the LC Receptacle: compatible with IEC 61000-4-3
- EMI/EMC compatible with FCC Part 15 Subpart B Rules, EN55022:2010
- Laser Eye Safety compatible with FDA 21CFR, EN60950-1& EN (IEC) 60825-1,2
- RoHS compliant with EU RoHS 2.0 directive 2015/863/EU

## Wavelength Guide (100GHz ITU-T Channel)

Channel #	Frequency (THz)	Center Wavelength (nm)
34	193.4	1550.12
35	193.5	1549.32
36	193.6	1548.51
37	193.7	1547.72
38	193.8	1546.92
39	193.9	1546.12
40	194.0	1545.32
41	194.1	1544.53
42	194.2	1543.73
43	194.3	1542.94
44	194.4	1542.14
45	194.5	1541.35
46	194.6	1540.56
47	194.7	1539.77
48	194.8	1538.98
49	194.9	1538.19
50	195.0	1537.40
51	195.1	1536.61
52	195.2	1535.82
53	195.3	1535.04
54	195.4	1534.25
55	195.5	1533.47
56	195.6	1532.68
57	195.7	1531.90
58	195.8	1531.12
59	195.9	1530.33
60	196.0	1529.55
61	196.1	1528.77

## Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Maximum Supply Voltage	V <sub>cc3</sub>	-0.5	3.6	V
	V <sub>cc5</sub>	-0.5	6	V
Storage Temperature	T <sub>S</sub>	-40	85	°C
Operating Temperature	T <sub>O</sub>	0	70	°C
Operating Humidity	RH	5	95	%
Receiver power	R <sub>MAX</sub>		-7	dBm
Maximum bitrate	B <sub>max</sub>	9.95	11.3	Gbps

## Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage	V <sub>cc3</sub>	3.135	3.30	3.465	V	
	V <sub>cc5</sub>	4.75	5.0	5.25	V	
Power Supply Current	I <sub>cc3</sub>			750	mA	
Power Supply Current	I <sub>cc5</sub>			500	mA	
Power Dissipation	P <sub>D</sub>			3500	mW	
<b>Transmitter</b>						
Differential data input swing	V <sub>in,pp</sub>	120		1000	mVp-p	
Input differential impedance	Z <sub>in</sub>		100		Ω	
Tx_Disable, P_Down/RST	V <sub>IH</sub>	2.0		V <sub>CC3</sub> +0.3	V	
	V <sub>IL</sub>	-0.3		0.8	V	
Transmit Disable Assert Time				10	us	
<b>Receiver</b>						
Differential data output swing	V <sub>out,pp</sub>	340		850	mVp-p	1
Output differential impedance	Z <sub>in</sub>		100		Ω	
Data Output Rise Time, Fall Time	t <sub>r</sub> , t <sub>f</sub>	24			ps	2
Rx_LOS, Mod_NR, Interrupt	V <sub>OH</sub>	V <sub>CCHOST</sub> -0.5		V <sub>CCHOST</sub> +0.3	V	3
	V <sub>OL</sub>	0		0.4	V	3

### Notes:

1. Internally AC coupled but requires an external 100Ω differential termination.
2. 20–80%.
3. Loss of Signal is an open collector output. Should be pulled up with a 4.7kΩ-10kΩ resistor on the host board.

## Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
<b>Transmitter</b>						
Launch Average Optical Power	P <sub>O</sub>	1		+4	dBm	1
Center Wavelength Range	λ <sub>c</sub>	1528.77		1563.86	nm	
Center Wavelength Spacing			100		GHz	
Center Wavelength Tolerance	Δλ <sub>c</sub>	-100		100	pm	
Extinction Ratio	EX	9			dB	2
Spectral Width (-20dB)	Δλ			0.3	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Average Optical Power (Laser Off)	P <sub>OFF</sub>			-30	dBm	1
Eye Diagram	ITU-T G.691 SDH STM-64 L-64.2 compatible					2
<b>Receiver</b>						
Center Wavelength	λ <sub>c</sub>	1528		1565	nm	
Receiver Sensitivity @ 9.953Gb/s	S			-26.0	dBm	3
Receiver Overload (P <sub>avg</sub> )	P <sub>OL</sub>	-7.0			dBm	3
Optical Return Loss	ORL	27			dB	
LOS De-Assert	LOS <sub>D</sub>			-27	dBm	
LOS Assert	LOS <sub>A</sub>	-38			dBm	
LOS Hysteresis		0.5			dB	

### Notes:

1. The optical power is launched into 9/125μm SMF.
2. Measured with a PRBS 2<sup>31</sup>-1 test pattern @ 9.953Gbps.
3. Measured with worst ER; 1550nm; PRBS 2<sup>31</sup>-1 test pattern @ 9.953Gb/s, BER<10<sup>-12</sup>.

## Pin Descriptions

Pin	Symbol	Name/Descriptions	Ref.
1	GND	Module Ground	
2	Vee5	(not required)	
3	MOD_DESEL	Module De-select; When Held low allows the module to respond to 2-wire serial interface. LVTTTL-I	
4	/INTERRUPT	Interrupt; Indicates presence of an important condition which can be read via the 2-wire serial interface. LVTTTL-O	2
5	TX_DIS	Transmitter Disable. Logic1 indicates laser output disabled, LVTTTL-I	
6	VCC5	+5V Power Supply (Not required)	
7	GND	Module Ground	1
8	VCC3	+3.3V Power Supply	
9	VCC3	+3.3V Power Supply	
10	SCL	2-Wire Serial Interface Clock. LVTTTL-I	2
11	SDA	2-Wire Serial Interface Data Line. LVTTTL-I/O	2
12	MOD_Abs	Indicates Module is not present. Grounded in the Module. LVTTTL-O	2
13	MOD_NR	Module Not Ready; Indicating Module Operational Fault. Open-collector. LVTTTL-O	2
14	RX_LOS	Loss of Signal indication. Logic 1 indicates loss of Signal. Open-collector. LVTTTL-O	2
15	GND	Module Ground	1
16	GND	Module Ground	1
17	RD-	Receiver Inverted Data Output. CML-O	
18	RD+	Receiver Non-Inverted Data Output. CML-O	
19	GND	Module Ground	1
20	VCC2	+1.8V Power Supply (Not required).	3
21	P_DOWN/RST	Power down; When high, requires the module to limit power consumption to 1.5W or below. 2-Wire serial interface must be functional in the low power mode. LVTTTL-I Reset; The falling edge initiates a complete reset of the module including the 2-wire serial interface, equivalent to a power cycle. LVTTTL-I	
22	VCC2	+1.8V Power Supply (Not required)	3
23	GND	Module Ground	1
24	REFCLK+	Reference Clock (Not required)	
25	REFCLK-	Reference Clock (Not required)	
26	GND	Module Ground	1
27	GND	Module Ground	1
28	TD-	Transmitter Inverted Data Input. CML-I	
29	TD+	Transmitter Non-Inverted Data Input. CML-I	
30	GND	Module Ground	1

**Notes:**

1. Module ground pins GND are isolated from the module case and chassis ground within the module.
2. Open collector; should be pulled up with 4.7K-10Kohms to a voltage between 3.15V and 3.6V on the host board.
3. The pins are open within module.



Pin-out of connector Block on Host board

### Recommended Circuit Schematic



### Mechanical Specifications

Small Form Factor Pluggable (XFP) transceivers are compatible with the dimensions defined by the XFP Multi-Sourcing Agreement (MSA).



## EEPROM Information

### Management Interface

XFP 2-wire serial interface is specified in the Chapter 4 of the XFP MSA specification. The XFP 2-wire serial interface is used for serial ID, digital diagnostics, and certain control functions. The 2-wire serial interface is mandatory for all XFP modules. The 2-wire serial interface address of the XFP module is 1010000X(A0h). In order to access to multiple modules on the same 2-wire serial bus, the XFP has a MOD\_DESEL(module deselect pin). This pin (which is pull high or deselected in the module) must be held low by the host to select of interest and allow communication over 2-wire serial interface. The module must not respond to or accept 2-wire serial bus instructions unless it is selected.

### XFP Management Interface

XFP Management interface is specified in the Chapter 5 of the XFP MSA specification. The Figure 1 shows the structure of the memory map. The normal 256 Byte address space is divided into lower and upper blocks of 128 Bytes. The lower block of 128 Byte is always directly available and is used for the diagnostics and control functions that must be accessed repeatedly. Multiple blocks of memories are available in the upper 128 Bytes of the address space. These are individually addressed through a table select Byte which the user enters into a location in the lower address space. The upper address space tables are used for less frequently accessed functions and control space for future standards definition.

EEPROM memory map specific data field description is as below:





**About Us:**

Proline Options is one of North America's leading providers of transceivers and high speed cabling. With a reputation for quality, tested products that cover the connectivity spectrum, Proline Options has a solution for you regardless of the specification.

At Proline Options, every product is tested in its intended application - never batch or spec tested only. We run bandwidth, distance and IOS network tests. We have documented an impressive 0.03% failure rate over the last 10 years. To continue this rate of success we invest millions annually in our own on-site testing lab.



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