

QDD-400G-LR8-40-PRO

Juniper Networks® QDD-400G-LR8-40 Compatible TAA Compliant 400GBase-ER8 PAM4 QSFP-DD Transceiver (SMF, 1270nm to 1330nm, 0 to 70C, LC)

Features

- Compliant with IEEE std 802.3cn-2019
- Compliant with QSFP-DD CMIS Rev 4.0
- Compliant with QSFP-DD MSA HW Rev 5.1
- Maximum link length of 40km on Single Mode Fiber (SMF)
- 8x50G PAM4 retimed 400GAUI-8 electrical interface
- Power dissipation <14W
- Class 1/1M Laser
- Operating Case Temperature 0 to 70 Celsius
- I2C management interface
- Duplex LC receptacles
- RoHS Compliant and Lead-Free



Applications:

- 400GBase Ethernet
- Access and Enterprise

Product Description

This Juniper Networks® QDD-400G-LR8-40 compatible QSFP-DD transceiver provides 400GBase-ER8 throughput up to 40km over single-mode fiber (SMF) using a wavelength of 1270nm to 1330nm via an LC connector. It is guaranteed to be 100% compatible with the equivalent Juniper Networks® transceiver. This easy to install, hot swappable transceiver has been programmed, uniquely serialized and data-traffic and application tested to ensure that it will initialize and perform identically. Digital optical monitoring (DOM) support is also present to allow access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

Proline's transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S. – made or designated country end products.



Regulatory Compliance

- ESD to the Electrical PINs: compatible with MIL-STD-883E Method 3015.4
- ESD to the LC Receptacle: compatible with IEC 61000-4-3
- EMI/EMC compatible with FCC Part 15 Subpart B Rules, EN55022:2010
- Laser Eye Safety compatible with FDA 21CFR, EN60950-1& EN (IEC) 60825-1,2
- RoHS compliant with EU RoHS 2.0 directive 2015/863/EU

Absolute Maximum Ratings

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Notes |
|------------------------------------|------------------|-------|---------|----------------------|------|-------|
| Storage Temperature | T _s | -40 | | 85 | °C | |
| Maximum Supply Voltage | V _{cc} | -0.5 | | 3.6 | V | |
| Relative Humidity (non-condensing) | RH | 5 | | 95 | % | |
| Operating Case Temperature | T _{opr} | 0 | | 70 | °C | |
| Relative Humidity (non-condensing) | RH | 5 | | 85 | % | |
| Control Input Voltage | V _i | -0.3 | | V _{cc} +0.5 | V | |
| Control Output Current | I _o | -20 | | 20 | mA | |
| Signaling Speed per Lane | DRL | | 26.5625 | | GBd | |
| Operating Distance | | 0.002 | | 40 | km | 1 |

Notes:

1. Channel insertion loss is 18dB for 40km.

Electrical Characteristics (High Speed Signal- compliant with IEEE 802.3 400GAUI-8)

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|---|--------------------|----------------------|-----|----------------------|------|-------|
| Supply Voltage | V _{CC} | 3.135 | 3.3 | 3.465 | V | |
| Maximum Power Dissipation | P _D | | | 14 | W | |
| Maximum Power Dissipation, Low Power Mode | P _{DLP} | | | 1.5 | W | |
| Instantaneous peak current at hot plug | I _{CC_IP} | | | 5600 | mA | |
| Sustained peak current at hot plug | I _{CC_SP} | | | 4620 | mA | |
| Control Input Voltage High | V _{IH} | V _{CC} *0.7 | | V _{CC} +0.3 | V | |
| Control Input Voltage Low | V _{IL} | -0.3 | | V _{CC} *0.3 | V | |
| Two Wire Serial Interface Clock Rate | | | | 400 | kHz | |
| Power Supply Noise | | | | 66 | mVpp | |
| Rx Differential Data Output Load | | | 100 | | Ohm | |
| Transmitter | | | | | | |
| AC Common- mode output Voltage (RMS) | | | | 17.5 | mV | |
| Differential Output Voltage | | | | 900 | mV | |
| Near end Eye Height, differential | | 70 | | | mV | |
| Far-end Eye height, differential | | 30 | | | mV | |
| Eye width Far end pre-cursor ratio | | | | 2.5 | % | |
| Differential Termination Mismatch | | | | 10 | % | |
| Transition Time (min, 20% to 80%) | | 9.5 | | | ps | |
| DC common mode Voltage | | -350 | | 2850 | mV | |
| Receiver | | | | | | |
| Differential pk-pk input Voltage tolerance | | 900 | | | mV | |
| Differential termination mismatch | | | | 10 | % | |
| Single-ended voltage tolerance range | | -0.4 | | 3.3 | V | |
| DC common mode Voltage | | -350 | | 2850 | mV | |
| Low Speed Signal (compliant with QSFP-DD HW Rev 5.1) | | | | | | |
| Module output SCL and SDA | V _{OL} | 0 | | 0.4 | V | |
| Module Input SCL and SDA | V _{IL} | -0.3 | | V _{CC} *0.3 | V | |
| | V _{IH} | V _{CC} *0.7 | | V _{CC} +0.5 | V | |
| InitMode, ResetL and ModSelL | V _{IL} | -0.3 | | 0.8 | V | |
| | V _{IH} | 2 | | V _{CC} +0.3 | V | |
| IntL | | 0 | | 0.4 | V | |
| | | V _{CC} -0.5 | | V _{CC} +0.3 | V | |

Optical Characteristics

| Parameter | Symbol | Min | Typical | Max | Unit | Notes | |
|---|------------|----------------|---------|---------|---------|-------|--|
| Transmitter | | | | | | | |
| Transmit wavelengths | L0 | λ_{c0} | 1272.55 | 1273.55 | 1274.54 | nm | |
| | L1 | λ_{c1} | 1276.89 | 1277.89 | 1278.89 | nm | |
| | L2 | λ_{c2} | 1281.25 | 1282.26 | 1283.27 | nm | |
| | L3 | λ_{c3} | 1285.65 | 1286.67 | 1287.68 | nm | |
| | L4 | λ_{c4} | 1294.53 | 1295.56 | 1296.59 | nm | |
| | L5 | λ_{c5} | 1299.02 | 1300.06 | 1301.09 | nm | |
| | L6 | λ_{c6} | 1303.54 | 1304.59 | 1305.63 | nm | |
| | L7 | λ_{c7} | 1308.09 | 1309.14 | 1310.19 | nm | |
| Side Mode Suppression Ratio | SMSR | 30 | | | dB | | |
| Total Average Launch Power | AOPT | | | 14.6 | dBm | | |
| Average Launch Power, each lane | AOPL | 0.6 | | 5.6 | dBm | 1 | |
| Outer Optical Modulation Amplitude (OMA_{outer}), each Lane | TOMA | 2.4 | | 6.4 | dBm | | |
| Difference in Launch Power between any two Lanes (OMA_{outer}) | DT OMA | | | 4 | dB | | |
| Launch Power in OMA_{outer} minus TDECQ, each lane | TOMA,TDECQ | 1 | | | dBm | | |
| Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each lane | TDECQ | | | 3.4 | dB | | |
| TDECQ-10log₁₀(Ceg) | | | | 3.4 | dB | | |
| Average Launch Power of OFF Transmitter, each lane | TOFF | | | -30 | dBm | | |
| Extinction Ratio | ER | 6 | | | dB | | |
| RIN_{15OMA} | RIN | | | -132 | dB/Hz | 1 | |
| Optical Return Loss Tolerance | ORL | | | 15 | dB | | |
| Transmitter Reflectance | TR | | | -26 | dB | 2 | |
| Receiver | | | | | | | |
| Receiver wavelengths | L0 | λ_{c0} | 1272.55 | 1273.55 | 1274.54 | nm | |
| | L1 | λ_{c1} | 1276.89 | 1277.89 | 1278.89 | nm | |
| | L2 | λ_{c2} | 1281.25 | 1282.26 | 1283.27 | nm | |
| | L3 | λ_{c3} | 1285.65 | 1286.67 | 1287.68 | nm | |
| | L4 | λ_{c4} | 1294.53 | 1295.56 | 1296.59 | nm | |
| | L5 | λ_{c5} | 1299.02 | 1300.06 | 1301.09 | nm | |
| | L6 | λ_{c6} | 1303.54 | 1304.59 | 1305.63 | nm | |
| | L7 | λ_{c7} | 1308.09 | 1309.14 | 1310.19 | nm | |
| Damage Threshold, each Lane | AOPD | -3.4 | | | dBm | | |

| | | | | | | |
|---|--------|------|------|-----------------------|-----|---|
| Average Receive Power, each Lane | AOPR | 18.6 | | -4.4 | dBm | |
| Receiver Power (OMAouter), each Lane | OMAR | | | -3.6 | dBm | |
| Difference in Receiver Power between any two Lanes (OMAouter) | DR_OMA | | | 5.8 | dB | |
| Receiver Reflectance | RR | | | -26 | dB | |
| Receiver Sensitivity (OMAouter), each Lane | SOMA | - | | Max(-16.1, SECQ-17.5) | dBm | 3 |
| Stressed Receiver Sensitivity (OMAouter), each Lane | SRS | | | -14.1 | dBm | 4 |
| Conditions of stressed receiver sensitivity test: | | | | | | |
| Stressed eye closure for PAM4 (SECQ), lane under test | | | 3.4 | | dB | |
| SECQ-10log10(Ceg), lane under test | | | | 3.4 | dB | |
| OMAouter of each aggressor lane | | | -8.3 | | dBm | |

Notes:

1. Average launch power, each lane (min) is informative and not the principle of signal strength
2. Transmitter reflectance is defined looking into the transmitter
3. Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with SECQ of 1.4 dB.
4. Measured with conformance test signal at TP3 for the BER = 2.4×10^{-4}

Timing for Soft Control and Status Functions

| Parameter | Symbol | Min | Max | Unit | Notes |
|-------------------------|-------------------|-----|------|------|-------------|
| MgmtInit Duration | | | 2000 | ms | |
| ResetL Assert Time | t_reset_init | 10 | | μs | |
| IntL Assert Time | ton_IntL | | 200 | ms | |
| IntL Deassert Time | toff_IntL | | 500 | μs | |
| Rx LOS Assert Time | ton_losf | | 100 | ms | |
| Flag Assert Time | ton_flag | | 200 | ms | |
| Mask Assert Time | ton_mask | | 100 | ms | |
| Mask Deassert Time | toff_mask | | 100 | ms | |
| Module Select Wait Time | ModSelL Wait Time | | N/A | | Not support |

I/O Timing for Squelch and Disable

| Parameter | Symbol | Min | Max | Unit | Notes |
|--------------------------------------|-------------|-----|------|------|---------------------|
| Rx Squelch Assert Time | ton_Rxsq | | 50 | ms | |
| Tx Squelch Assert Time | ton_Txsq | | 400 | ms | |
| Tx Squelch Deassert Time | toff_Txsq | | 1500 | ms | Based on Modulation |
| Tx Disable Assert Time (fast mode) | ton_Txdisf | | 3 | ms | |
| Tx Disable Deassert Time (fast mode) | toff_Txdisf | | 10 | ms | |
| Rx Output Disable Assert Time | ton_Rxdis | | 100 | ms | |
| Rx Output Disable Deassert Time | toff_Rxdis | | 100 | ms | |
| Squelch Disable Assert Time | ton_sqdis | | N/A | ms | Not support |
| Squelch Disable Deassert Time | toff_sqdis | | N/A | ms | Not support |

Digital Diagnostics

| Parameter | Range | Accuracy | Unit | Calibration |
|------------------------------|---------------|----------|------|-------------|
| Temperature | 0 to 70 | ±3 | °C | Internal |
| Voltage | 0 to VCC | 0.1 | V | Internal |
| Tx Bias Current (Each Lane) | 0 to 100 | 10% | mA | Internal |
| Tx Output Power (Each Lane) | -0.6 to +5.6 | ±3 | dB | Internal |
| Rx Receive Power (Each Lane) | -18.6 to -4.4 | ±3 | dB | Internal |

Pin Descriptions

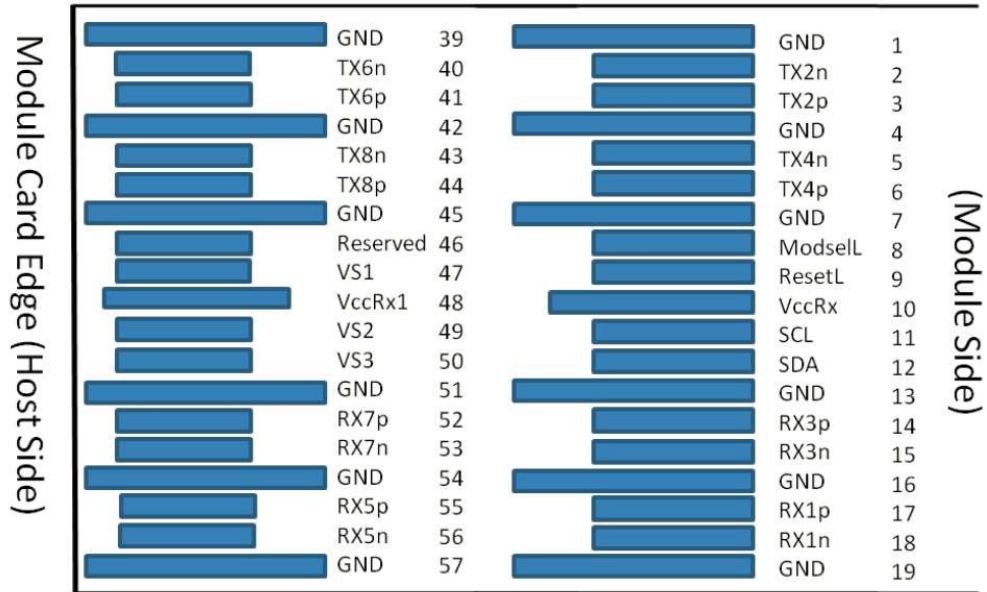
| Pin | Logic | Symbol | Name/Descriptions |
|-----|-------------|----------|-------------------------------------|
| 1 | | GND | Ground |
| 2 | CML-I | Tx2n | Transmitter Inverted Data Input |
| 3 | CML-I | Tx2p | Transmitter Non-inverted Data Input |
| 4 | | GND | Ground |
| 5 | CML-I | Tx4n | Transmitter Inverted Data Input |
| 6 | CML-I | Tx4p | Transmitter Non-inverted Data Input |
| 7 | | GND | Ground |
| 8 | LVTTTL-I | ModSelL | Module Select |
| 9 | LVTTTL-I | ResetL | Module Reset |
| 10 | | VccRx | +3.3V Power Supply Receiver |
| 11 | LVC MOS-I/O | SCL | 2-wire serial interface clock |
| 12 | LVC MOS-I/O | SDA | 2-wire serial interface data |
| 13 | | GND | Ground |
| 14 | CML-O | Rx3p | Receiver Non-inverted Data Output |
| 15 | CML-O | Rx3n | Receiver Inverted Data Output |
| 16 | | GND | Ground |
| 17 | CML-O | Rx1p | Receiver Non-inverted Data Output |
| 18 | CML-O | Rx1n | Receiver Inverted Data Output |
| 19 | | GND | Ground |
| 20 | | GND | Ground |
| 21 | CML-O | Rx2n | Receiver Inverted Data Output |
| 22 | CML-O | Rx2p | Receiver Non-inverted Data Output |
| 23 | | GND | Ground |
| 24 | CML-O | Rx4n | Receiver Inverted Data Output |
| 25 | CML-O | Rx4p | Receiver Non-inverted Data Output |
| 26 | | GND | Ground |
| 27 | LVTTTL-O | ModPrsL | Module Present |
| 28 | LVTTTL-O | IntL | Interrupt |
| 29 | | VccTx | +3.3V Power Supply Transmitter |
| 30 | | Vcc1 | +3.3V Power Supply |
| 31 | LVTTTL-I | InitMode | Initialization mode |
| 32 | | GND | Ground |
| 33 | CML-I | Tx3p | Transmitter Non-inverted Data Input |
| 34 | CML-I | Tx3n | Transmitter Inverted Data Input |
| 35 | | GND | Ground |
| 36 | CML-I | Tx1p | Transmitter Non-inverted Data Input |
| 37 | CML-I | Tx1n | Transmitter Inverted Data Input |
| 38 | | GND | Ground |
| 39 | | GND | Ground |

| | | | |
|----|-------|----------|-------------------------------------|
| 40 | CML-I | Tx6n | Transmitter Inverted Data Input |
| 41 | CML-I | Tx6p | Transmitter Non-inverted Data Input |
| 42 | | GND | Ground |
| 43 | CML-I | Tx8n | Transmitter Inverted Data Input |
| 44 | CML-I | Tx8p | Transmitter Non-inverted Data Input |
| 45 | | GND | Ground |
| 46 | | Reserved | |
| 47 | | VS1 | Module Vendor Specific 1 |
| 48 | | VccRx1 | 3.3V Power Supply |
| 49 | | VS2 | Module Vendor Specific 2 |
| 50 | | VS3 | Module Vendor Specific 3 |
| 51 | | GND | Ground |
| 52 | CML-O | Rx7p | Receiver Non-inverted Data Output |
| 53 | CML-O | Rx7n | Receiver Inverted Data Output |
| 54 | | GND | Ground |
| 55 | CML-O | Rx5p | Receiver Non-inverted Data Output |
| 56 | CML-O | Rx5n | Receiver Inverted Data Output |
| 57 | | GND | Ground |
| 58 | | GND | Ground |
| 59 | CML-O | Rx6n | Receiver Inverted Data Output |
| 60 | CML-O | Rx6p | Receiver Non-inverted Data Output |
| 61 | | GND | Ground |
| 62 | CML-O | Rx8n | Receiver Inverted Data Output |
| 63 | CML-O | Rx8p | Receiver Non-inverted Data Output |
| 64 | | GND | Ground |
| 65 | | NC | Not connected |
| 66 | | Reserved | |
| 67 | | VccTx1 | 3.3V Power Supply |
| 68 | | Vcc2 | 3.3V Power Supply |
| 69 | | Reserved | |
| 70 | | GND | Ground |
| 71 | CML-I | Tx7p | Transmitter Non-inverted Data Input |
| 72 | CML-I | Tx7n | Transmitter Inverted Data Input |
| 73 | | GND | Ground |
| 74 | CML-I | Tx5p | Transmitter Non-inverted Data Input |
| 75 | CML-I | Tx5n | Transmitter Inverted Data Input |
| 76 | | GND | Ground |

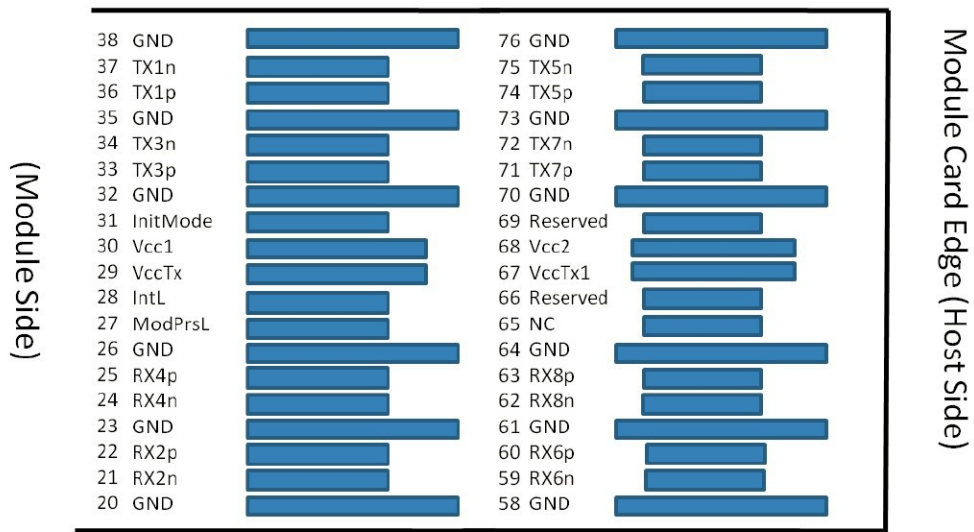
Notes:

1. Circuit ground is internally isolated from chassis ground.

MSA Compliant Connector



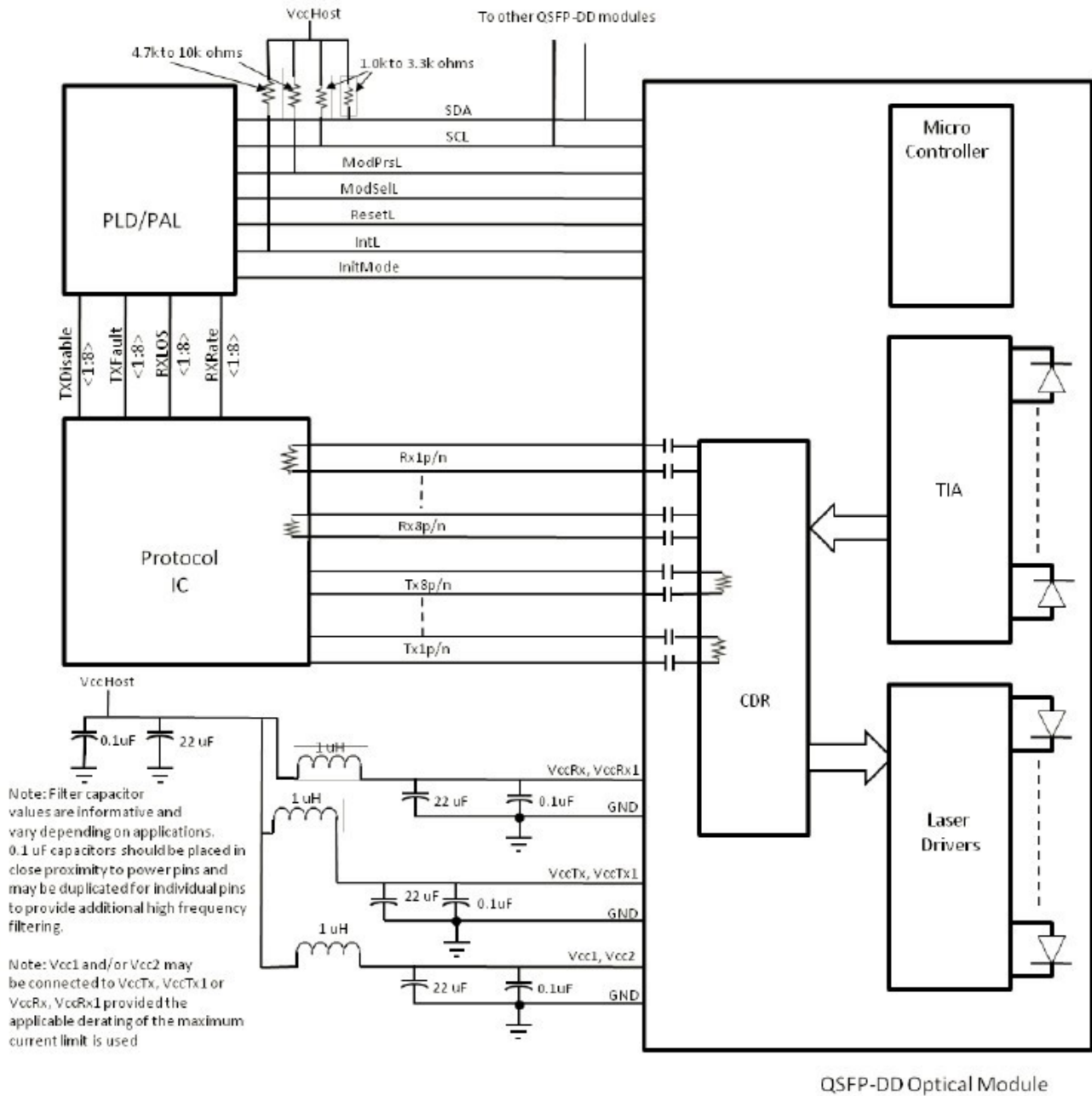
Bottom side viewed from bottom



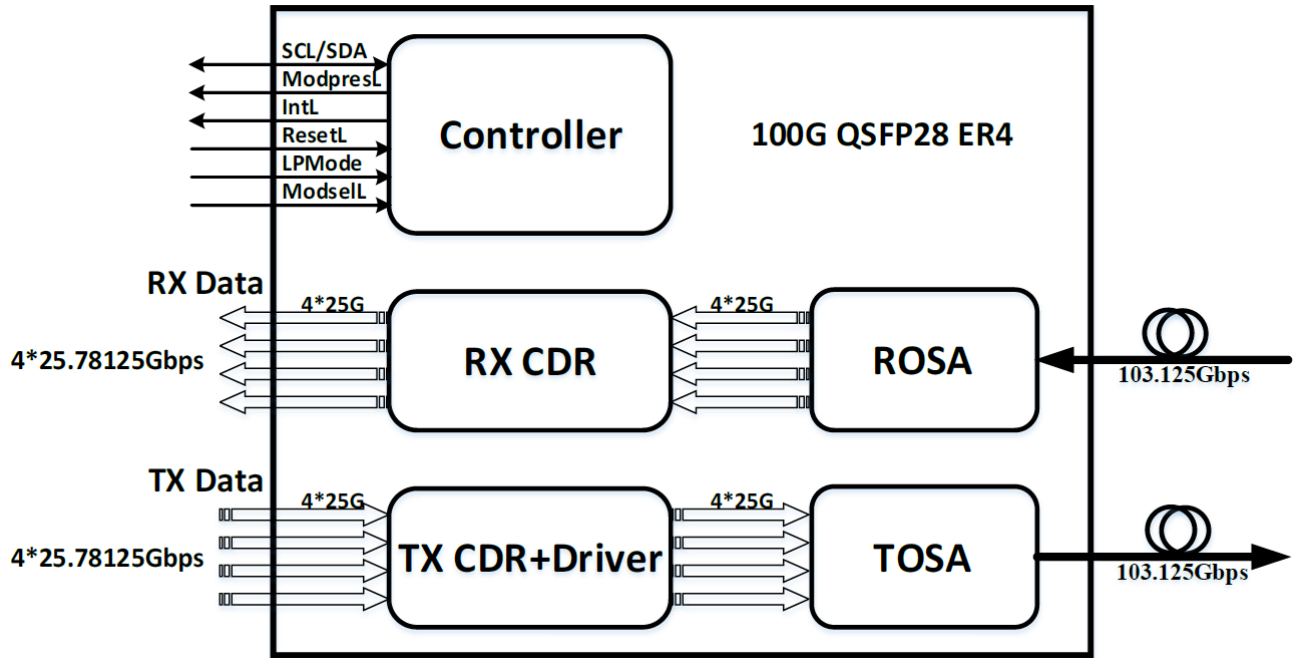
Top side viewed from top

Pin definitions of the module high speed inputs/outputs

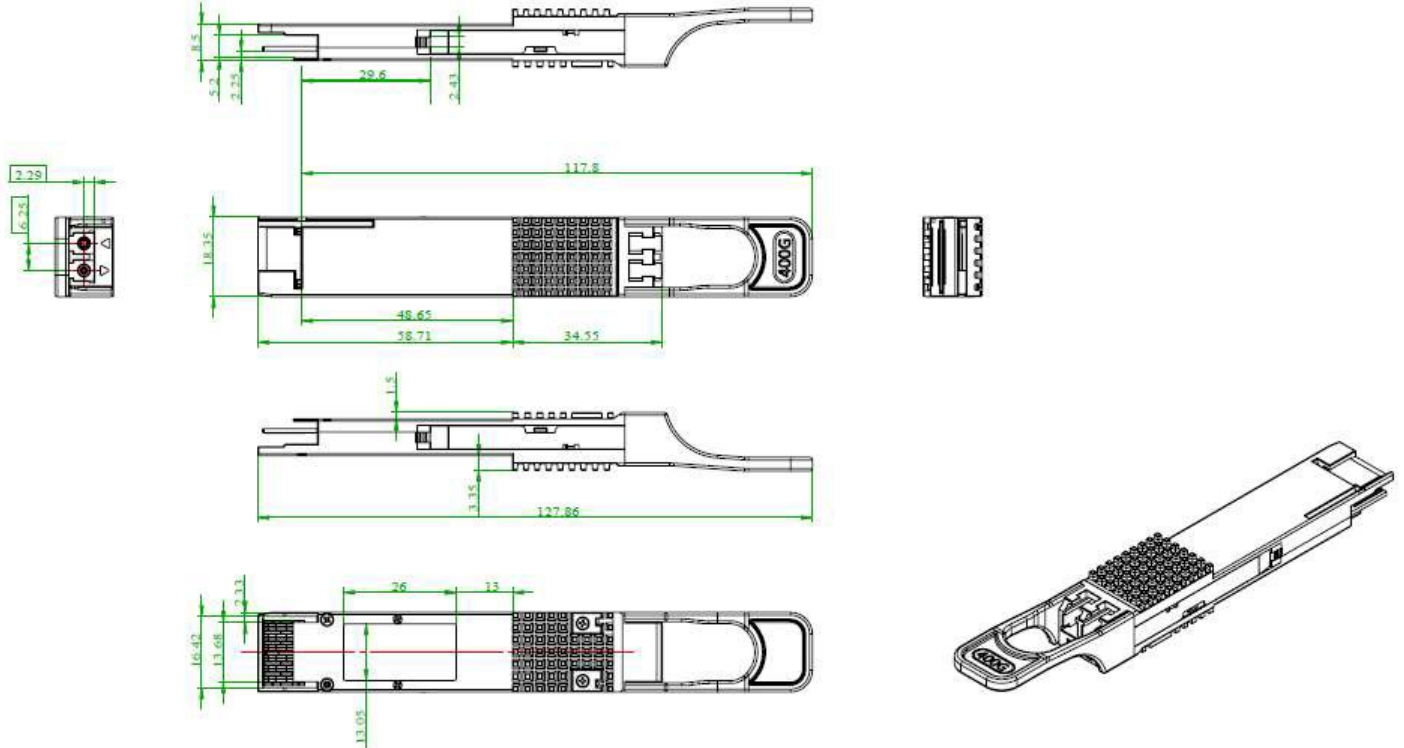
Recommended QSFP-DD Host Board Schematic



Transceiver Block Diagram



Mechanical Specifications



About Us:

Proline Options is one of North America's leading providers of transceivers and high speed cabling. With a reputation for quality, tested products that cover the connectivity spectrum, Proline Options has a solution for you regardless of the specification.

At Proline Options, every product is tested in its intended application - never batch or spec tested only. We run bandwidth, distance and IOS network tests. We have documented an impressive 0.03% failure rate over the last 10 years. To continue this rate of success we invest millions annually in our own on-site testing lab.



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