

PRO-QSFPDD-EDFA-DUAL-20DB-C

Cisco® Compatible QSFP-DD Dual Pluggable EDFA Booster amplifier for DWDM, Duplex LC, Input power -20dBm to 0dBm, Nominal gain +20dB

Features:

- QSFP-DD MSA Compliant Electrical and Mechanical Interfaces
- QSFP-DD Dual Pluggable EDFA Booster and Amplifier
- C-Band 8-Channel DWDM Amplification
- 20dB Nominal Gain with Automatic Gain Control
- Duplex LC Connector
- Power Dissipation Maximum of 3W
- Operating Temperature: 0 to 70 Celsius
- RoHS compliant and lead-free



Product Description:

This Cisco® compatible QSFP-DD dual pluggable EDFA booster amplifier offers a optical input range and provides a +20dB nominal gain to a C-Band DWDM link. The dual pluggable EDFA connects to a composite DWDM link via an LC connector. It is configured for Automatic Gain Control (AGC) by default and can be further configured via CLI prompt in supported hosts or by our coding and tuning system.

General Specifications

Parameter	Symbol	Min.	Тур.	Max.	Unit
Supply Voltage	Vcc	3.13	3.3	3.46	VDC
Storage Temperature	Tstg	-40		85	°C
Operating Temperature	Тс	-5	25	70	°C
Humidity	Н	10		85	%
Power Dissipation	P _{DISS}			3	W

Optical Characteristics

Parameter	Symbol	Min.	Тур.	Max.	Unit	Notes
Operating Wavelength	λ	1542		1554	nm	
Channel Number		1		8		
Input Power	P_in	-20		-11	dBm	
Output Power	P_out		9	14	dBm	
Optical Power Shutdown	P_off			-30	dBm	1
Output Power Variation	ΔΡΟυΤ	-0.5		0.5	dB	
Gain			20		dB	
Gain Flatness	GF			1.0	dB	2
Gain Accuracy	ΔG	-1		1	dB	
Noise Figure	NF_PA			8	dB	
	NF_BA			10	dB	
Transient Performance				3	dB	3
Return Loss	RL	40			dB	
VOA Attenuation Range				30	dB	

Notes:

- 1. Assert when both BA and PA input signals are at loss.
- 2. Peak-to-peak.
- 3. 3dB add/drop.
- 4. PA and BA share the same value if not specified.

Pin Descriptions

Pin	Logic	Symbol	Name/Description	Plug Sequence	Notes
1		GND	Module Ground.	1B	1
2	CML-I	Tx2-	Not Connected.	3B	
3	CML-I	Tx2+	Not Connected.	3B	
4		GND	Module Ground.	1B	1
5		Tx4-	Not Connected.	3B	
6		Tx4+	Not Connected.	3B	
7		GND	Module Ground.	1B	1
8	LVTTL-I	ModSelL	Module Select.	3B	
9	LVTTL-I	ResetL	Module Reset.	3B	
10		VccRx	+3.3V Receiver Power Supply.	2B	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock.	3B	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data.	3B	
13		GND	Module Ground.	1B	1
14	CML-O	Rx3-	Not Connected.	3B	
15	CML-O	Rx3+	Not Connected.	3B	
16		GND	Module Ground.	1B	1
17	CML-O	Rx1-	Not Connected.	3B	
18	CML-O	Rx1+	Not Connected.	3B	
19		GND	Module Ground.	1B	1
20		GND	Module Ground.	1B	1
21	CML-O	Rx2-	Not Connected.	3B	
22	CML-O	Rx2+	Not Connected.	3B	
23		GND	Module Ground.	1B	1
24	CML-O	Rx4-	Not Connected.	3B	
25	CML-O	Rx4+	Not Connected.	3B	
26		GND	Module Ground.	1B	1
27	LVTTL-O	ModPrsL	Module Present.	3B	
28	LVTTL-O	IntL/RxLOS	Interrupt/Optional RxLOS.	3B	
29		VccTx	+3.3V Transmitter Power Supply.	2B	2
30		Vcc1	+3.3V Power Supply.	2B	2
31	LVTTL-I	LPMode/TxDis	Optional Tx Disable.	3B	
32		GND	Module Ground.	1B	1
33	CML-I	Tx3-	Not Connected.	3B	
34	CML-I	Tx3+	Not Connected.	3B	
35		GND	Module Ground.	1B	1

36	CML-I	Tx1-	Not Connected.	3B	
37	CML-I	Tx1+	Not Connected.	3B	
38		GND	Module Ground.	1B	1
39		GND	Module Ground.	1A	1
40	CML-I	Tx6-	Not Connected.	3A	
41	CML-I	Tx6+	Not Connected.	3A	
42		GND	Module Ground.	1A	1
43	CML-I	Tx8-	Not Connected.	3A	
44	CML-I	Tx8+	Not Connected.	3A	
45		GND	Module Ground.	1A	1
46	LVCMOS/CML-I	P/VS4	Not Connected.	3A	4
47	LVCMOS/CML-I	P/VS1	Not Connected.	3A	4
48		VccRx1	+3.3V Power Supply.	2A	2
49	LVCMOS/CML-O	P/VS2	Not Connected.	3A	4
50	LVCMOS/CML-O	P/VS3	Not Connected.	3A	4
51		GND	Module Ground.	1A	1
52	CML-O	Rx7-	Not Connected.	3A	
53	CML-O	Rx7+	Not Connected.	3A	
54		GND	Module Ground.	1A	1
55	CML-O	Rx6-	Not Connected.	3A	
56	CML-O	Rx6+	Not Connected.	3A	
57		GND	Module Ground.	1A	1
58		GND	Module Ground.	1A	1
59	CML-O	Rx6-	Not Connected.	3A	
60	CML-O	Rx6+	Not Connected.	3A	
61		GND	Module Ground.	1A	1
62	CML-O	Rx8-	Not Connected.	3A	
63	CML-O	Rx8+	Not Connected.	3A	
64		GND	Module Ground.	1A	1
65		NC	Not Connected.	3A	3
66		Reserved	For Future Use.	3A	3
67		VccTx1	+3.3V Transmitter Power Supply.	2A	2
68		Vcc2	+3.3V Power Supply.	2A	2
69	LVCMOS-I	ePPS/Clock	Not Connected.	3A	5
70		GND	Module Ground.	1A	1
71	CML-I	Tx7-	Not Connected.	3A	
72	CML-I	Tx7+	Not Connected.	3A	

73		GND	Module Ground.	1A	1
74	CML-I	Tx5-	Not Connected.	3A	
75	CML-I	Tx5+	Not Connected.	3A	
76		GND	Module Ground.	1A	1

Notes:

- 1. QSFP-DD uses common ground (GND) for all signal and supply (power). All are common within the QSFP-DD module, and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane. Each connector GND contact is rated for a maximum current of 500mA.
- 2. VccRx, VccRx1, Vcc1, Vcc2, VccTx, and VccTx1 shall be applied concurrently. Supply requirements defined for the host side of the Host Card Edge Connector. For power classes 4 and above, the module differential loading of input voltage pins must not result in exceeding contact current limits. Each connector Vcc contact is rated for a maximum current of 1500mA.
- 3. Reserved and Not Connected pins are recommended to be terminated with $10k\Omega$ to ground on the host. Pin 65 (Not Connected) shall be left unconnected within the module.
- 4. Full definitions of the P/VSx signals currently under development. On new designs, unused P/VSx signals are recommended to be terminated on the host with $10k\Omega$.
- 5. ePPS/Clock, if not used, is recommended to be terminated with 50Ω to ground on the host.
- 6. Plug Sequences specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, and 3B. Contact sequence A will make, then break, contact with additional QSFP-DD pins. Sequence 1A and 1B will then occur simultaneously, followed by 2A and 2B, followed by 3A and 3B.

Electrical Pin-Out Details

23

22

21

GND

RX2p

RX2n

GND

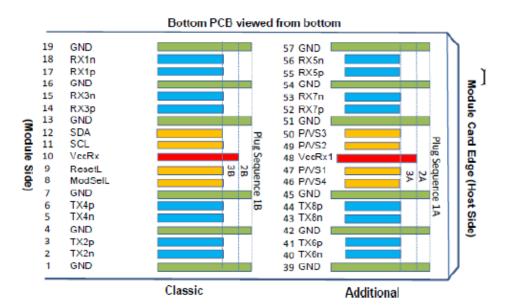
Top PCB viewed from top 38 GND 76 GND 37 TX1n 75 TX5n 74 TX5p 36 TX1p GND 73 GND 35 Module Card Edge (Host Side) 34 TX3n 72 TX7n 33 71 TX7p ТХ3р 32 GND 70 GND (Module Side) 31 LPMode/TxDis 69 ePPS/Clock Plug Sequence 30 Vcc1 68 Vcc2 29 VccTx 67 VccTx1 28 27 IntL/RxLOS 66 Reserved ModPraL 65 NC 26 GND 64 GND RX4p 25 63 RX8p 5 RX4n 62 RX8n 24

61 GND

60 RX6p

59 RX6n

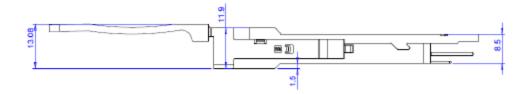
58 GND

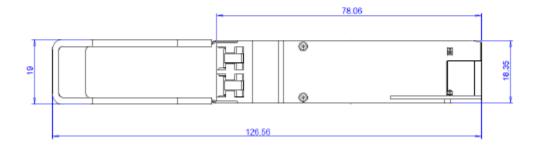


Product Sketch Map



Mechanical Specifications

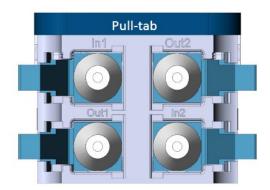




Notes:

- 1. All dimensions are in mm.
- 2. This module's design is QSFP-DD Multi-Sourcing Agreement (MSA) compliant.

Optical Port Layout



Parameter	Specification	Connector
In1	PA Input	LC/UPC
Out1	PA Output	LC/UPC
In2	BA Input	LC/UPC
Out2	BA Output	LC/UPC

About Us:

Proline Options is one of North America's leading providers of transceivers and high speed cabling. With a reputation for quality, tested products that cover the connectivity spectrum, Proline Options has a solution for you regardless of the specification.

At Proline Options, every product is tested in its intended application - never batch or spec tested only. We run bandwidth, distance and IOS network tests. We have documented an impressive 0.03% failure rate over the last 10 years. To continue this rate of success we invest millions annually in our own on-site testing lab.



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