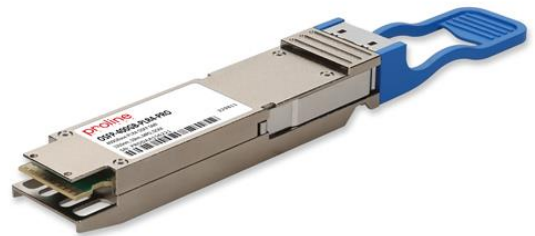


OSFP-400GB-PLR4-PRO

MSA and TAA Compliant 400GBase-PLR4 OSFP Transceiver (SMF, 1310nm, 10km, DOM, CMIS 4.0, 0 to 70C, MPO)

Features

- OSFP MSA Compliant
- Supports up to 425Gbps
- 400GAUI-8 Interface Compliance Defined by IEEE802.3bs
- Single-Mode Fiber
- MPO-12 Connector
- 8x53.125Gbps (PAM4) Electrical Interface
- CMIS 4.0 or Later
- PIN and TIA Array on Receiver Side
- Hot Pluggable
- Commercial Temperature 0 to 70 Celsius
- Metal with Lower EMI
- RoHS Compliant and Lead-Free



Applications:

- 400GBase Ethernet

Product Description

This MSA Compliant OSFP transceiver provides 400GBase-PLR4 throughput up to 10km over single-mode fiber (SMF) using a wavelength of 1310nm via an MPO connector. It is built to MSA standards and is uniquely serialized and data-traffic and application tested to ensure that they will integrate into your network seamlessly. Digital optical monitoring (DOM) support is also present to allow access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

Proline's transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S. – made or designated country end products.



Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage	V _{cc}	-0.5	3.3	3.6	V	
Storage Temperature	T _{stg}	-40		85	°C	
Operating Case Temperature	T _c	0		70	°C	1
Relative Humidity	RH	5		55	%	
Operating Relative Humidity	RH			65	%	
Power Dissipation	P _{DISS}			10	W	

Notes:

1. The position of the case temperature measurement is shown in the Mechanical Specifications section.
2. Exceeding the Absolute Maximum Ratings table may cause permanent damage to the device. This is just an emphasized rating and does not involve the functional operation of the device that exceeds the specifications of this technical specification under these or other conditions. Long-term operation under Absolute Maximum Ratings will affect the reliability of the device.

Electrical Characteristics

Parameter	Symbol / Test Point	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage	V _{cc}	3.135	3.3	3.465	V	
Power Supply Total Current				3190	mA	
Power Supply Noise				50	mVp-p	1
Electrical Signal Rate Per Channel			26.5625		GBd	2
In-Rush Instantaneous Peak Current	I _{Peak}			4000	mA	
In-Rush Current (DI/Dt)	I _{Inrush}			100	mA/us	
Power Consumption				10	W	
AC Coupling Internal Capacitor			0.1		μF	
Transmitter High-Speed Electrical Characteristics						
Signaling Rate Per Lane (Range)	TP1		26.5625 ± 100ppm		GBd	
Data Input Voltage – Single-Ended		-0.5		V _{cc} +0.5	V	
Data Input Voltage – Differential				0.8	V	3
Differential Peak-to-Peak Input Voltage Tolerance	TP1a	900			mV	
Differential Return Loss (Minimum)	TP1		Equation (83E-5)		dB	4
Common-Mode to Differential Return Loss (Minimum)	TP1		Equation (83E-6)		dB	4
Differential Termination Mismatch	TP1			10	%	
Single-Ended Voltage Tolerance Range	TP1a	-0.4		3.3	V	
DC Common-Mode Voltage	TP1	-350		2850	mV	5

Module Stressed Input Test	TP1a		120E.3.4.1			6, 7
Eye Width			0.22		UI	
Applied Peak-to-Peak Sinusoidal Jitter			Table 120E-6			6
Eye Height			32		mV	
Receiver High-Speed Electrical Characteristics						
Signaling Rate Per Lane (Range)	TP4		26.5625 ± 100ppm		GBd	
Receiver Differential Data Output Load		100			Ω	
AC Common-Mode Output Voltage (Maximum, RMS)				17.5	mV	
Differential Peak-to-Peak Output Voltage Tolerance	TP4			900	mV	
Near-End ESMW (Eye Symmetry Mask Width)	TP4		0.265		UI	
Near-End Height Differential	TP4	90			mV	
Far-End ESMW (Eye Symmetry Mask Width)	TP4		0.2		UI	
Far-End Eye Height Differential	TP4	30			mV	
Differential Output Return Loss (Minimum)	TP4		Equation (83E-2)		dB	4
Common- to Differential-Mode Conversion Return Loss (Minimum)	TP4		Equation (83E-3)		dB	4
Differential Termination Mismatch	TP4			10	%	
Transition Time (20-80%)	TP4	9.5			ps	
DC Common-Mode Voltage	TP4	-0.35		2.85	V	

Notes:

1. Power Supply Noise is defined as the peak-to-peak noise amplitude over the frequency range at the host supply side of the recommended power supply filter with the module and recommended filter in place. Voltage levels including peak-to-peak noise are limited to the recommended operating range of the associated power supply.
2. 400GAUI-8 operation with host-generated FEC. The transmitter must receive pre-coded FEC signals from the host ASIC.
3. This is the maximum voltage that can be applied across the differential inputs without damaging the input circuitry. The damage threshold of the module input shall be at least 1600mV peak-to-peak differential.
4. Per IEEE 802.3bm specification.
5. DC Common-Mode Voltage is generated by the host. Specification includes the effects of ground offset voltage.
6. Per IEEE 802.3bs specification.
7. Module Stressed Input Tolerance is measured using the procedure defined in 120E-3.4.1.

Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Optical Signal Rate Per Channel			53.125		GBd	1
Fiber Length (9 μ m SMF)			10		km	2
Transmitter						
Signaling Speed Per Lane			106.25		Gbps	
Modulation Format		PAM4				
Center Wavelength	λ C	1304.5	1311	1317.5	nm	
Side-Mode Suppression Ratio	SMSR	30			dB	
Extinction Ratio	ER	3.5			dB	
Average Launch Power	Pavg	-1.9		4.8	dBm	3
OMA Per Lane				5	dBm	
Launch Power in OMA-TDECQ	ER \geq 4.5dB		-1.2		dBm	
	ER $<$ 4.5dB		-1.1		dBm	
TDECQ (PAM4)				3.3	dB	
SECQ				3.3	dB	
RIN _{15.1} OMA				-132	dB/Hz	
Average Launch Power of Off Transmitter	Poff			-30	dBm	
Optical Return Loss Tolerance	ORLT			15.6	dB	
Transmitter Reflectance				-26	dB	
Transmitter Transition Time				17	ps	
Receiver						
Signaling Speed Per Lane			106.25		Gbps	
Center Wavelength	λ C	1305.5	1311	1317.5	nm	
Damage Threshold	Rxdmg	5.8			dBm	
Average Receiver Power Per Lane	RxAVG	-8.2		4.8	dBm	
Receive Power (OMA) Per Lane	RxOMA			5	dBm	
Receiver Sensitivity (OMA) Per Lane	SenOMA			Max. (-6.1, TECQ-7.5)	dBm	4
Stressed Receiver Sensitivity (OMA) Per Lane	SRS			-4.1	dBm	
LOS Assert (Average)	LOSA	-15			dBm	
LOS De-Assert (Average)	LOSD			-10	dBm	
LOS Hysteresis	LOSH	0.5			dB	
RSSI Accuracy		-2		+2	dB	
Receiver Reflectance				-26	dB	

Notes:

- 400G LR8 operation with host-generated FEC. The transmitter must receive pre-coded FEC signals from the host ASIC.

2. 9 μ m SMF. The maximum link distance is based on an allocation of 1dB of attenuation and 3dB total connection and splice loss. The loss of a single connection shall not exceed 0.5dB.
3. Average launch power, per lane (minimum), is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
4. Receiver sensitivity, @<4.6dBm, for Tx with TDECQ<1.4dB; @<SECQ-6, for Tx with 3.4dB \ge TDECQ \ge 1.4dB.

Pin Descriptions

Pin	Logic	Symbol	Name/Description	Plug Sequence	Notes
1		GND	Module Ground.	1	1
2	CML-I	Tx2+	Transmitter Non-Inverted Data.	3	
3	CML-I	Tx2-	Transmitter Inverted Data.	3	
4		GND	Module Ground.	1	1
5	CML-I	Tx4+	Transmitter Non-Inverted Data.	3	
6	CML-I	Tx4-	Transmitter Inverted Data.	3	
7		GND	Module Ground.	1	1
8	CML-I	Tx6+	Transmitter Non-Inverted Data.	3	
9	CML-I	Tx6-	Transmitter Inverted Data.	3	
10		GND	Module Ground.	1	1
11	CML-I	Tx8+	Transmitter Non-Inverted Data.	3	
12	CML-I	Tx8-	Transmitter Inverted Data.	3	
13		GND	Module Ground.	1	1
14	LVC MOS-I/O	SCL	2-Wire Serial Interface Clock.	3	2
15		Vcc	+3.3V Power Supply.	2	
16		Vcc	+3.3V Power Supply.	2	
17	Multi-Level	LPWn/PRSn	Low-Power Mode/Module Present.	3	
18		GND	Module Ground.	1	1
19	CML-O	Rx7-	Receiver Inverted Data.	3	
20	CML-O	Rx7+	Receiver Non-Inverted Data.	3	
21		GND	Module Ground.	1	1
22	CML-O	Rx5-	Receiver Inverted Data.	3	
23	CML-O	Rx5+	Receiver Non-Inverted Data.	3	
24		GND	Module Ground.	1	1
25	CML-O	Rx3-	Receiver Inverted Data.	3	
26	CML-O	Rx3+	Receiver Non-Inverted Data.	3	
27		GND	Module Ground.	1	1
28	CML-O	Rx1-	Receiver Inverted Data.	3	
29	CML-O	Rx1+	Receiver Non-Inverted Data.	3	

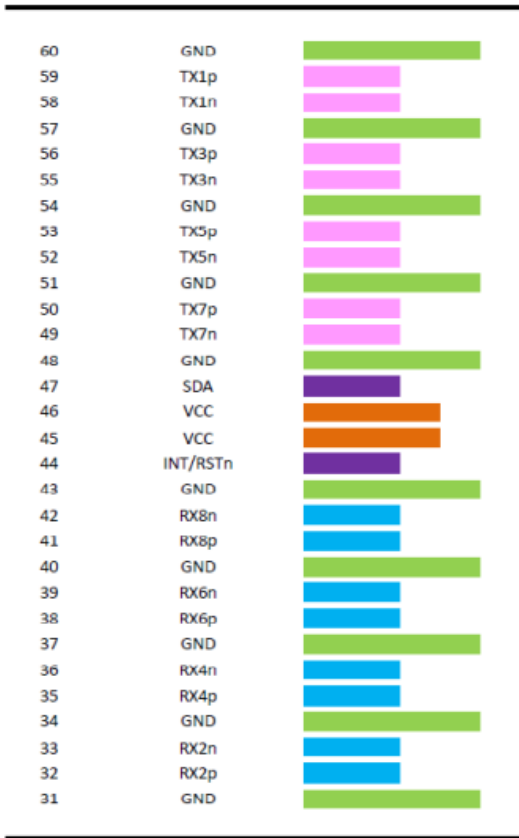
30		GND	Module Ground.	1	1
31		GND	Module Ground.	1	1
32	CML-O	Rx2+	Receiver Non-Inverted Data.	3	
33	CML-O	Rx2-	Receiver Inverted Data.	3	
34		GND	Module Ground.	1	1
35	CML-O	Rx4+	Receiver Non-Inverted Data.	3	
36	CML-O	Rx4-	Receiver Inverted Data.	3	
37		GND	Module Ground.	1	1
38	CML-O	Rx6+	Receiver Non-Inverted Data.	3	
39	CML-O	Rx6-	Receiver Inverted Data.	3	
40		GND	Module Ground.	1	1
41	CML-O	Rx8+	Receiver Non-Inverted Data.	3	
42	CML-O	Rx8-	Receiver Inverted Data.	3	
43		GND	Module Ground.	1	1
44	Multi-Level	INT/RSTn	Module Input/Module Reset.	3	
45		Vcc	+3.3V Power Supply.	2	
46		Vcc	+3.3V Power Supply.	2	
47	LVC MOS-I/O	SDA	2-Wire Serial Interface Data.	3	2
48		GND	Module Ground.	1	1
49	CML-I	Tx7-	Transmitter Inverted Data.	3	
50	CML-I	Tx7+	Transmitter Non-Inverted Data.	3	
51		GND	Module Ground.	1	1
52	CML-I	Tx5-	Transmitter Inverted Data.	3	
53	CML-I	Tx5+	Transmitter Non-Inverted Data.	3	
54		GND	Module Ground.	1	1
55	CML-I	Tx3-	Transmitter Inverted Data.	3	
56	CML-I	Tx3+	Transmitter Non-Inverted Data.	3	
57		GND	Module Ground.	1	1
58	CML-I	Tx1-	Transmitter Inverted Data.	3	
59	CML-I	Tx1+	Transmitter Non-Inverted Data.	3	
60		GND	Module Ground.	1	1

Notes:

1. OSFP uses common ground (GND) for all signals and supply (power). All are common within the OSFP module, and all module voltages are referenced to this potential unless otherwise noted.
2. Open-drain with pull-up resistor on the host.

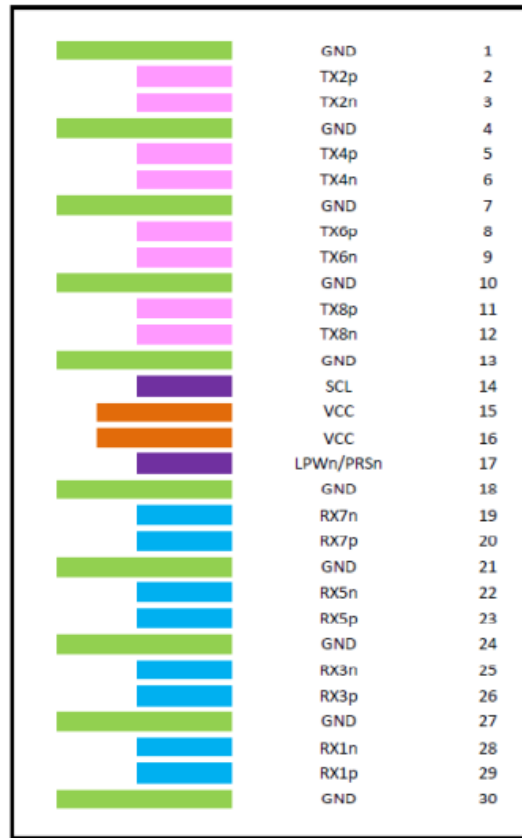
Electrical Pad Layout

Top Side (viewed from top)

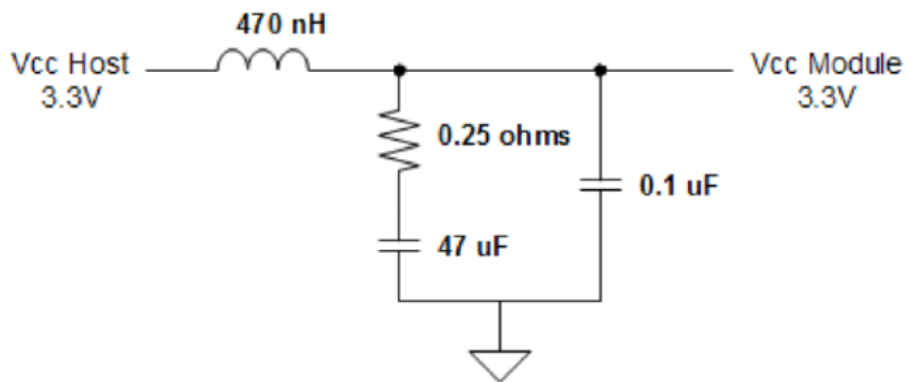


----- Module Card Edge -----

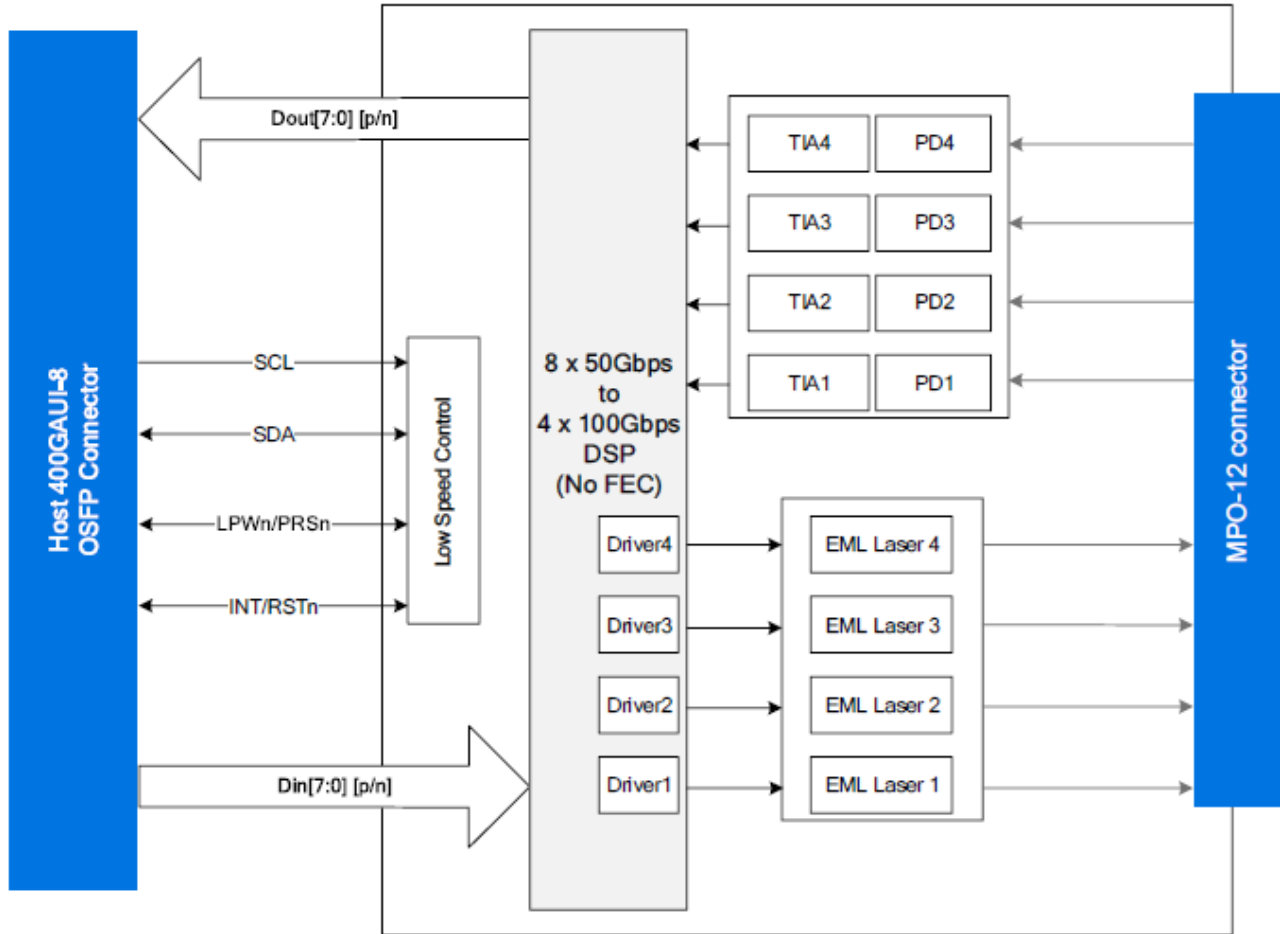
Bottom Side (viewed from bottom)



Recommended Host Board Power Supply Filter



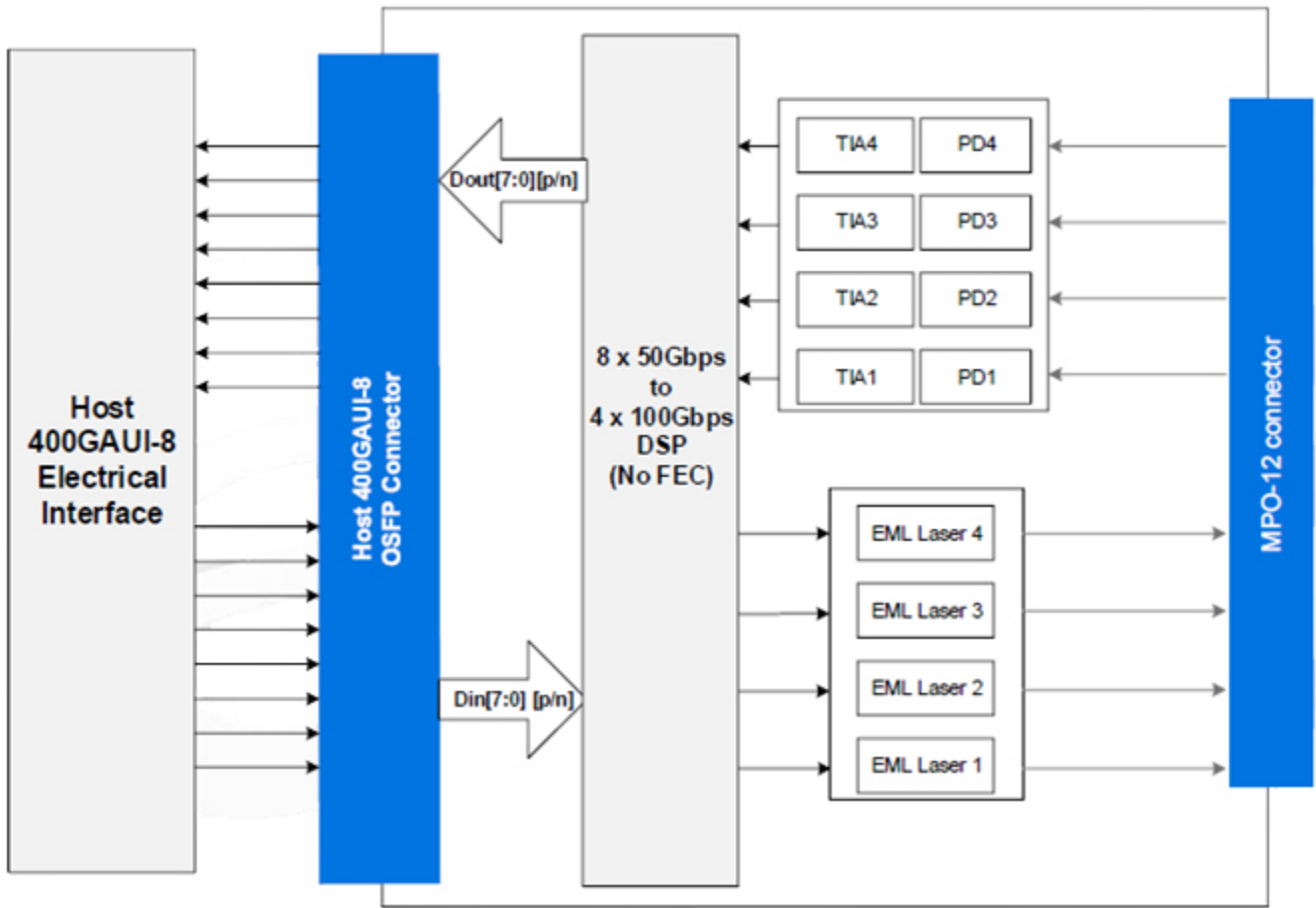
Transceiver Block Diagram



Notes:

1. The optical transmitter portion of the transceiver incorporates a 4x100Gbps 400GAUI-8 electrical input with Equalization (EQ) block, integrated electrical multiplexer, EML laser driver, diagnostic monitors, control and bias for the four EA modulator and single-mode laser source.
2. The optical receiver portion of the transceiver incorporates two optical de-multiplexers, eight PIN photodiodes, trans-impedance amplifiers (TIA), integrated de-multiplexer, and 4x100G 400GAUI-8 compliant electrical output blocks.

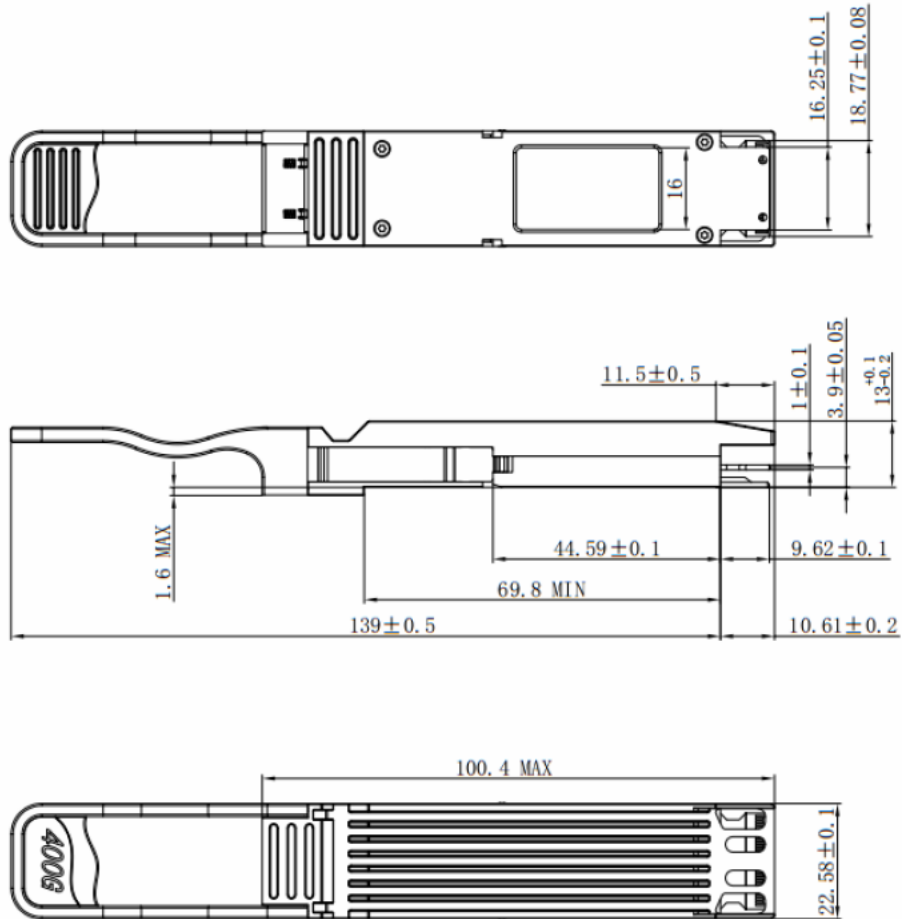
Application Reference Diagram



Notes:

1. The interface between the OSFP module and an ASIC/SerDes is shown above. The high-speed signal lines are internally AC coupled, and the electrical inputs are internally terminated to 100Ω differential. All transmitter and receiver electrical channels are compliant to module 400GAUI-8 specifications per IEEE 802.3bs.

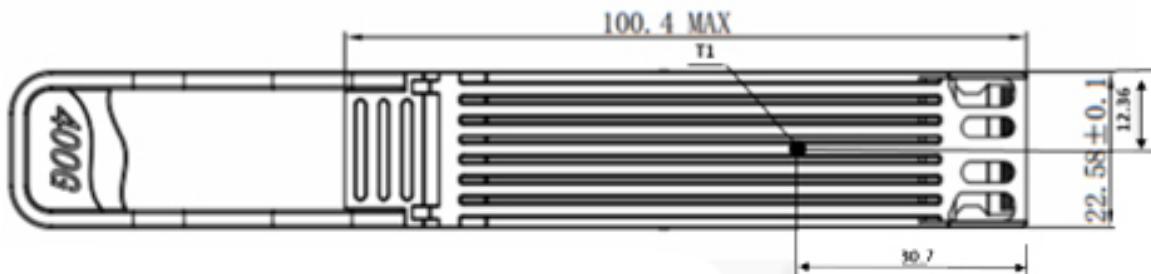
Mechanical Specifications



Notes:

1. All dimensions are in mm.
2. For safety and protection of the host system, the power to each OSFP module may be protected by an electronic circuit breaker on the host board which is enabled with the H_PRSn signal such that power is only enabled when the module is fully engaged into the OSFP connector.

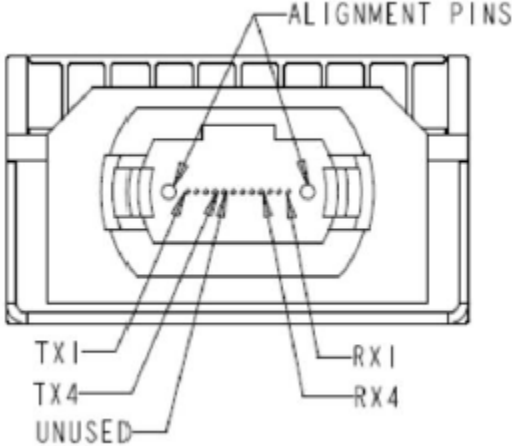
Case Temperature Measurement Point



Notes:

1. All dimensions are in mm.

Module Optical Interface (Looking into the Optical Port)



Notes:

- 1. The optical interface port is an MPO-12 connector.

About Us:

Proline Options is one of North America's leading providers of transceivers and high speed cabling. With a reputation for quality, tested products that cover the connectivity spectrum, Proline Options has a solution for you regardless of the specification.

At Proline Options, every product is tested in its intended application - never batch or spec tested only. We run bandwidth, distance and IOS network tests. We have documented an impressive 0.03% failure rate over the last 10 years. To continue this rate of success we invest millions annually in our own on-site testing lab.



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