MMA4Z00-NS-PRO

Mellanox® MMA4Z00-NS Compatible TAA Compliant 800GBase-2xSR4 PAM4 OSFP Transceiver (MMF, 850nm, 50m, DOM, CMIS 5.0, 0 to 70C, 2xMPO)

Features

- OSFP MSA Compliant
- 8x53.125GBd (PAM4) Electrical Interface
- Supports 850Gbps
- Commercial Temperature: 0 to 70 Celsius
- VCSEL Transmitter
- Dual MPO-12 Connector APC
- RoHS Compliant and Lead-Free
- PIN and TIA Array on the Receiver Side

Applications:

- 2x400GBase Ethernet
- 8x100GBase Ethernet

Product Description

This Mellanox® MMA4Z00-NS compatible OSFP transceiver provides 800GBase-2xSR4 throughput up to 50m over multi-mode fiber (MMF) using a wavelength of 850nm via a 2xMPO connector. It is guaranteed to be 100% compatible with the equivalent Mellanox® transceiver. This easy to install, hot swappable transceiver has been programmed, uniquely serialized and data-traffic and application tested to ensure that it will initialize and perform identically. Digital optical monitoring (DOM) support is also present to allow access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

Proline's transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S. – made or designated country end products.

TAA COMPLIANT

Rev. 021424

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage	Vcc	-0.5	3.3	3.6	V	
Storage Temperature	Tstg	-40		85	°C	
Operating Case Temperature	Tc	0		70	°C	1
Relative Humidity (non-condensing)	RH	5		85	%	
Fiber Length (OM3)				30	m	
Fiber Length (OM4)				50	m	

Notes:

1. The position of the case temperature measurement is shown in the Mechanical Specifications section.
2. Exceeding the Absolute Maximum Ratings table may cause permanent damage to the device. This is just an emphasized rating and does not involve the functional operation of the device that exceeds the specifications of this technical specification under these or other conditions. Long-term operation under Absolute Maximum Ratings will affect the reliability of the device.

Electrical Characteristics

Parameter		Symbol / Test Point	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage		Vcc	3.135	3.3	3.465	V	
Power Supply Total Current					3190	mA	
Power Supply Noise					25	mVpp	1
Receiver Differential Data Output Load				100		Ohm	
Transceiver Power Consumption					14	W	
Transceiver Power Supply Total Current					4242	mA	
AC Coupling Internal Capacitor				0.1		µF	
High-Speed Electrical Input Characteristics							
Signaling Rate Per Lane (Range)		TP1		53.125± 100ppm		GBd	
Differential Peak-Peak Input Voltage Tolerance		TP1a	750			mV	2
Peak-to-Peak AC Common-Mode Voltage Tolerance	**Low-frequency, VCM_{LF}**	TP1a	32			mV	
	Full-band, VCM_{FB}	TP1a	80			mV	
Differential-Mode to Common-Mode Return Loss, *RLcd*		TP1	Equation (120G-2)			dB	3
Effective Return Loss, ERL		TP1	8.5			dB	
Differential Termination Mismatch		TP1			10	%	
Single-Ended Voltage Tolerance Range		TP1a	-0.4		3.3	V	
DC Common-Mode Output Voltage		TP1	-350		2850	mV	4
Module Stressed Input Tolerance		TP1a					5

Pattern Generator Transition Time (Target)				9		ps	
Applied Peak-Peak Sinusoidal Jitter				Table 162-17			6
Eye Height (Target)				15		mV	
Vertical Eye Closure			12		12.5	dB	
Crosstalk Differential Peak-Peak Voltage				750		mV	
Crosstalk Transition Time	**Short Mode**			10		ps	
	Long Mode			15		ps	
High-Speed Electrical Output Characteristics							
Signaling Rate Per Lane (Range)		TP4		53.125± 100ppm		GBd	
Peak-to-Peak AC Common-Mode Voltage	**Low-frequency, VCM_{LF}**	TP4			32	mV	
	Full-band, VCM_{FB}	TP4			80	mV	
Differential Peak-to-Peak Output Voltage	**Short Mode**	TP4			600	mV	
	Long Mode	TP4			845	mV	
Eye Height		TP4	15			mV	
Vertical Eye Closure, VEC		TP4			12	dB	
Common to Differential Mode Conversion Return Loss, *RLdc*		TP4	Equation (120G-1)			mV	7
Effective Return Loss, ERL		TP4	8.5			dB	
Differential Termination Mismatch		TP4			10	%	
Transition Time (20% ~80%)		TP4	8.5			ps	
DC Common Mode Voltage Tolerance		TP4	-350		2850	mV	8

Notes:

1. Power Supply Noise is defined as the peak-to-peak noise amplitude over the frequency range at the host supply side of the recommended power supply filter with the module and recommended filter in place. Voltage levels including peak-to-peak noise are limited to the recommended operating range of the associated power supply. See recommended power supply filter figure on page 9.
2. With the exception to 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.
3. Equation (120G-2) refers to IEEE 803ck.
4. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.
5. Meets BER specified in 120G.1.1 of IEEE 802.3ck.
6. Table 162-17 refers to IEEE 802.3ck.
7. Equation (120G-1) refers to IEEE 802.3ck.
8. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

High-Speed Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter (@TP2 Test Point)						
Signaling Speed Per Lane	DR		53.125± 100ppm		Gbps	
Modulation Format			PAM4			
Center Wavelength	λC	842		868	nm	
RMS Spectral Width	△λrms			0.65	nm	1
Average Launch Power, Each Lane	Pavg	-4.6		4	dBm	
Outer Optical Modulation Amplitude (OMA_{outer}), Each Lane (Max)	POMA			3.5	dBm	
Outer Optical Modulation Amplitude (OMA_{outer}), Each Lane (min) for Max (TECQ, TDECQ) ≤1.8dB	POMA	-2.6			dBm	
Outer Optical Modulation Amplitude (OMA_{outer}), Each Lane (min) for 1.8<Max (TECQ, TDECQ) ≤4.4dB	POMA	-4.4+max (TECQ, TDECQ)			dBm	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each Lane	TDECQ			4.4	dB	
Transmitter Eye Closure for PAM4 (TECQ), each Lane	TECQ			4.4	dB	
Overshoot/Undershoot				29	%	
Transmitter Power Excursion, each Lane				2.3	dBm	
Extinction Ratio, each Lane	ER	2.5			dB	
Transmitter Transition Time, each Lane				17	ps	
Average Launch Power of OFF Transmitter, each Lane	Poff			-30	dBm	
$RIN_{12}OMA$	$RIN_{12}OMA$			-132	dB/Hz	
Optical Return Loss Tolerance	ORL			14	dB	
Encircled Flux	EF		≥86% at 19 μm ≤30% at 4.5 μm			2
Receiver (@TP3 Test Point)						
Signaling Speed Per Lane			53.125± 100ppm		Gbps	
Modulation Format			PAM4			
Center Wavelength	λ	842		948	nm	
Damage Threshold		5			dBm	3
Average Receiver Power, each Lane		-6.3		4	dBm	4
Receiver Reflectance				-15	dB	
Receiver Sensitivity (OMA_{outer}) for TECQ≤1.8dB	SEN			-4.4	dBm	
Receiver Sensitivity (OMA_{outer}) for 1.8<TECQ≤4.4dB	SEN			-6.2+TECQ	dBm	
LOS Assert	LOSA	-15			dBm	
LOS De-Assert	LOSD			-9	dBm	

Stressed Receiver Sensitivity (OMA_{outer}), each Lane			-1.8	dBm	dB	5
Conditions of Stressed Receiver Sensitivity Test (Note 6)						
Stressed Eye Closure for PAM4 (SECQ), Lane Under Test			4.4		dB	
OMA_{outer} of Each Aggressor Lane			3.5		dBm	

Notes:

1. RMS spectral width is the standard deviation of the spectrum.
2. If measured into type A1a.2 or type A1a.3, or A1a.4, 50um fiber, in accordance with IEC61280-1-4.
3. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level on one lane. The receiver does not have to operate correctly at this input power.
4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
5. Measured with conformance test signal at TP3 (see 167.8.14) for the BER specified in 167.1.1.
6. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Pin Descriptions

Pin	Logic	Symbol	Name/Description	Plug Sequence	Notes
1		GND	Module Ground.	1	1
2	CML-I	Tx2+	Transmitter Non-Inverted Data.	3	
3	CML-I	Tx2-	Transmitter Inverted Data.	3	
4		GND	Module Ground.	1	1
5	CML-I	Tx4+	Transmitter Non-Inverted Data.	3	
6	CML-I	Tx4-	Transmitter Inverted Data.	3	
7		GND	Module Ground.	1	1
8	CML-I	Tx6+	Transmitter Non-Inverted Data.	3	
9	CML-I	Tx6-	Transmitter Inverted Data.	3	
10		GND	Module Ground.	1	1
11	CML-I	Tx8+	Transmitter Non-Inverted Data.	3	
12	CML-I	Tx8-	Transmitter Inverted Data.	3	
13		GND	Module Ground.	1	1
14	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock.	3	2
15		Vcc	+3.3V Power Supply.	2	
16		Vcc	+3.3V Power Supply.	2	
17	Multi-Level	LPWn/PRSn	Low-Power Mode/Module Present.	3	
18		GND	Module Ground.	1	1
19	CML-O	Rx7-	Receiver Inverted Data.	3	

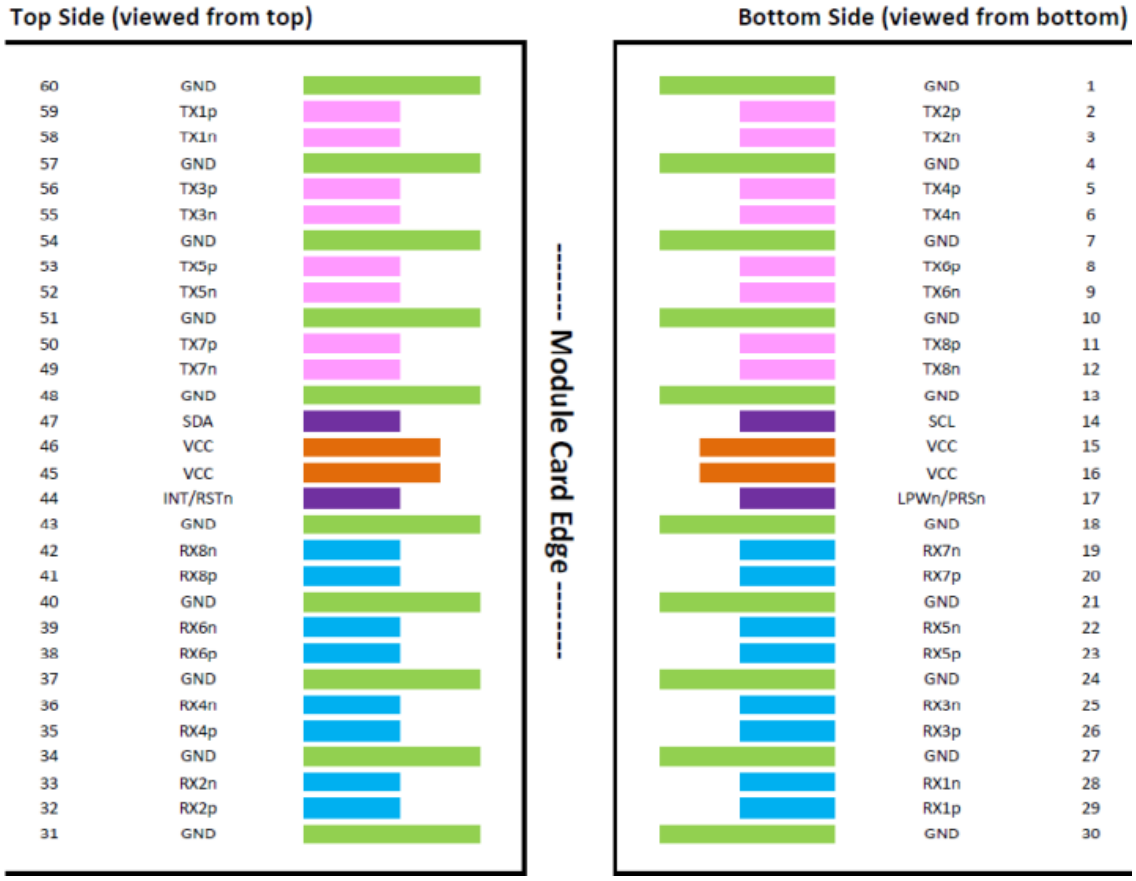
20	CML-O	Rx7+	Receiver Non-Inverted Data.	3	
21		GND	Module Ground.	1	1
22	CML-O	Rx5-	Receiver Inverted Data.	3	
23	CML-O	Rx5+	Receiver Non-Inverted Data.	3	
24		GND	Module Ground.	1	1
25	CML-O	Rx3-	Receiver Inverted Data.	3	
26	CML-O	Rx3+	Receiver Non-Inverted Data.	3	
27		GND	Module Ground.	1	1
28	CML-O	Rx1-	Receiver Inverted Data.	3	
29	CML-O	Rx1+	Receiver Non-Inverted Data.	3	
30		GND	Module Ground.	1	1
31		GND	Module Ground.	1	1
32	CML-O	Rx2+	Receiver Non-Inverted Data.	3	
33	CML-O	Rx2-	Receiver Inverted Data.	3	
34		GND	Module Ground.	1	1
35	CML-O	Rx4+	Receiver Non-Inverted Data.	3	
36	CML-O	Rx4-	Receiver Inverted Data.	3	
37		GND	Module Ground.	1	1
38	CML-O	Rx6+	Receiver Non-Inverted Data.	3	
39	CML-O	Rx6-	Receiver Inverted Data.	3	
40		GND	Module Ground.	1	1
41	CML-O	Rx8+	Receiver Non-Inverted Data.	3	
42	CML-O	Rx8-	Receiver Inverted Data.	3	
43		GND	Module Ground.	1	1
44	Multi-Level	INT/RSTn	Module Input/Module Reset.	3	
45		Vcc	+3.3V Power Supply.	2	
46		Vcc	+3.3V Power Supply.	2	
47	LVCMOS-I/O	SDA	2-Wire Serial Interface Data.	3	2
48		GND	Module Ground.	1	1
49	CML-I	Tx7-	Transmitter Inverted Data.	3	
50	CML-I	Tx7+	Transmitter Non-Inverted Data.	3	
51		GND	Module Ground.	1	1
52	CML-I	Tx5-	Transmitter Inverted Data.	3	
53	CML-I	Tx5+	Transmitter Non-Inverted Data.	3	
54		GND	Module Ground.	1	1
55	CML-I	Tx3-	Transmitter Inverted Data.	3	
56	CML-I	Tx3+	Transmitter Non-Inverted Data.	3	

57		GND	Module Ground.	1	1
58	CML-I	Tx1-	Transmitter Inverted Data.	3	
59	CML-I	Tx1+	Transmitter Non-Inverted Data.	3	
60		GND	Module Ground.	1	1

Notes:

1. OSFP uses common ground (GND) for all signals and supply (power). All are common within the OSFP module, and all module voltages are referenced to this potential unless otherwise noted.
2. Open-Drain with pull-up resistor on the host.

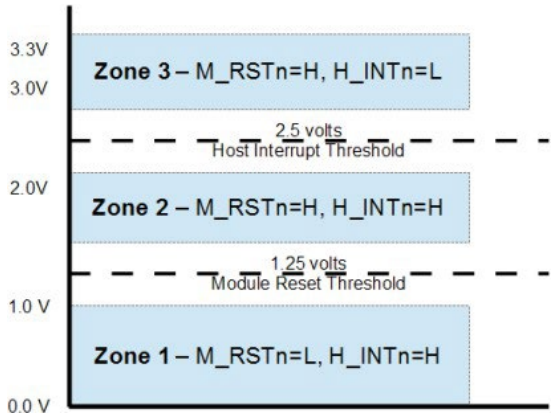
Electrical Pad Layout



INT/RSTn

INT/RSTn is a dual function signal that allows the module to raise an interrupt to the host and also allows the host to reset the module. The circuit shown in OSFP MSA Figure 11-3 enables multi-level signaling to provide direct signal control in both directions. Reset is an active low signal on the host which is translated to an active-low signal on the module. Interrupt is an active-high signal on the module which gets translated to an active-low signal on the host.

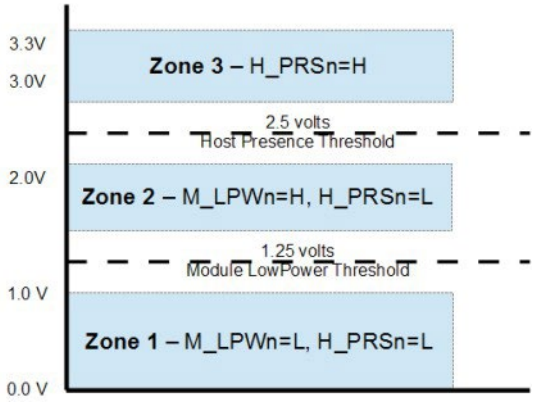
The INT/RSTn signal operates in 3 voltage zones to indicate the state of Reset for the module and Interrupt for the host. The figure below shows these 3 zones. The host uses a voltage reference at 2.5 volts to determine the state of the H_INTn signal and the module uses a voltage reference at 1.25V to determine the state of the M_RSTn signal.



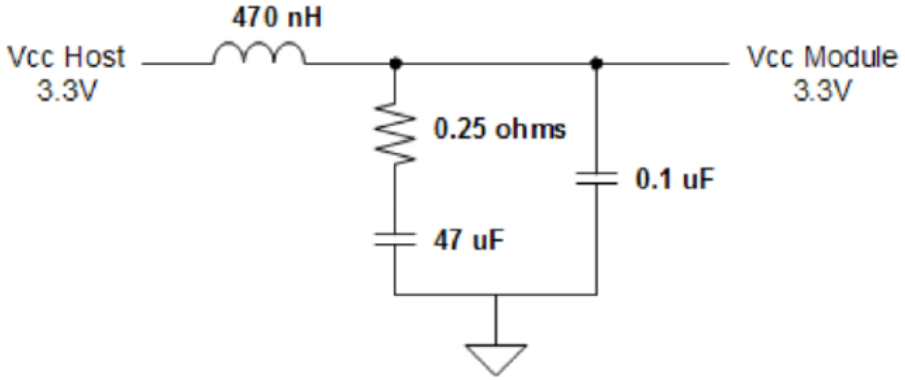
LPWn/PRSn

LPWn/PRSn is a dual function signal that allows the host to signal Low Power mode and the module to indicate Module Present. The circuit shown in OSFP MSA Figure 11-5 enables multi-level signaling to provide direct signal control in both directions. Low Power mode is an active-low signal on the host which gets converted to an active-low signal on the module. Module Present is controlled by a pull-down resistor on the module which gets converted to an active-low logic signal on the host.

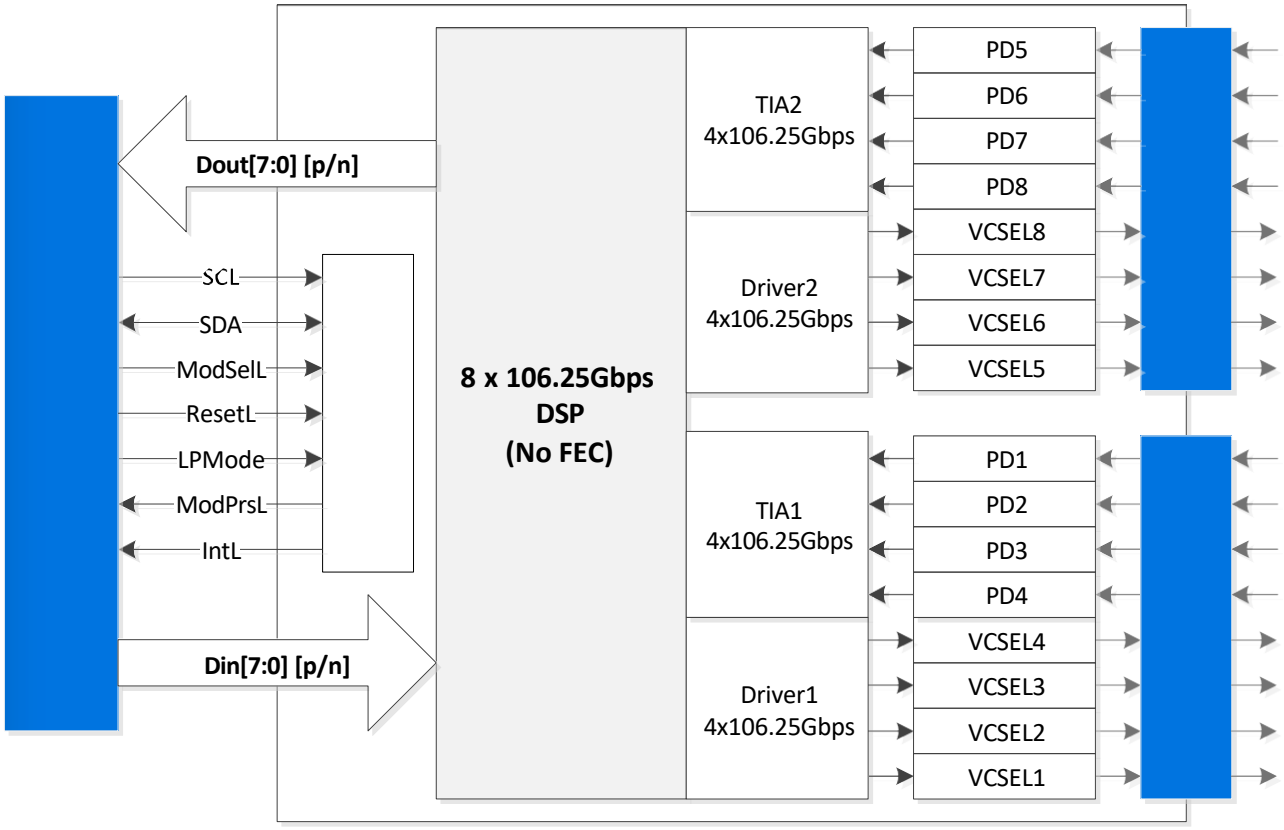
The LPWn/PRSn signal operates in 3 voltage zones to indicate the state of Low Power mode for the module and Module Present for the host. The figure below shows these 3 zones. The host uses a voltage reference at 2.5 volts to determine the state of the H_PRSn signal and the module uses a voltage reference at 1.25V to determine the state of the M_LPWn signal.



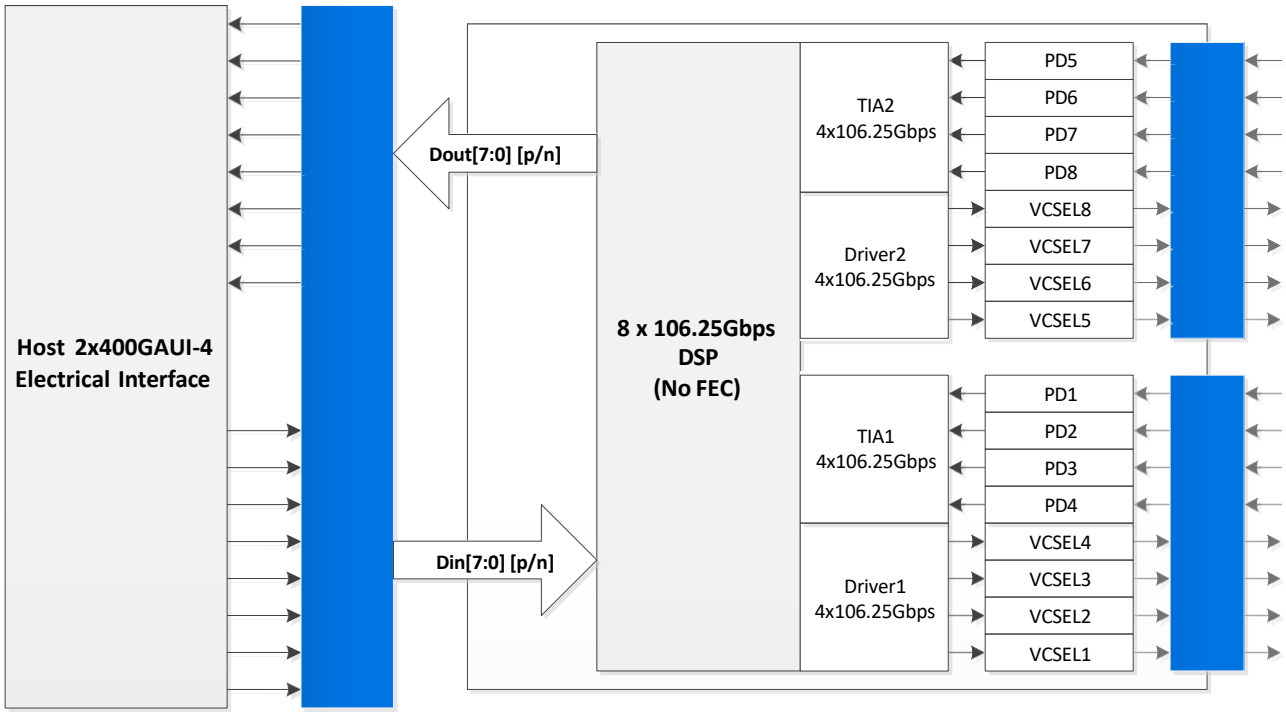
Recommended Host Board Power Supply Filter



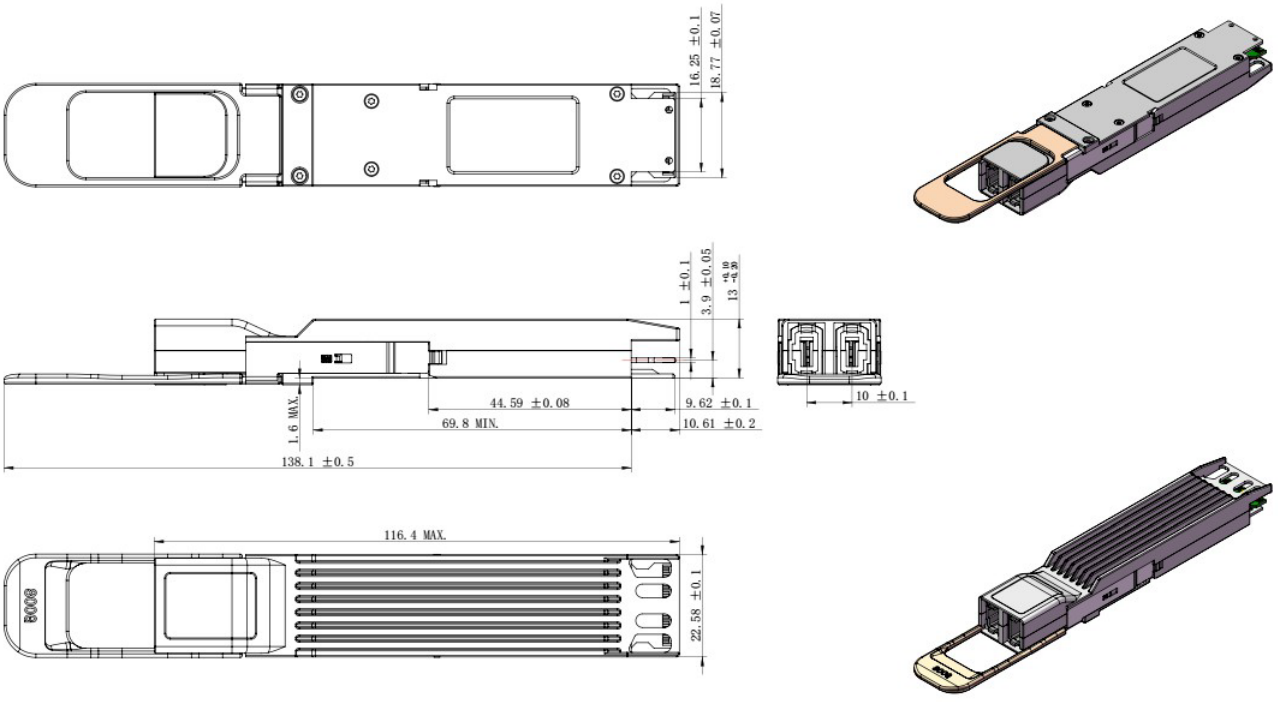
Transceiver Block Diagram



Application Reference Diagram

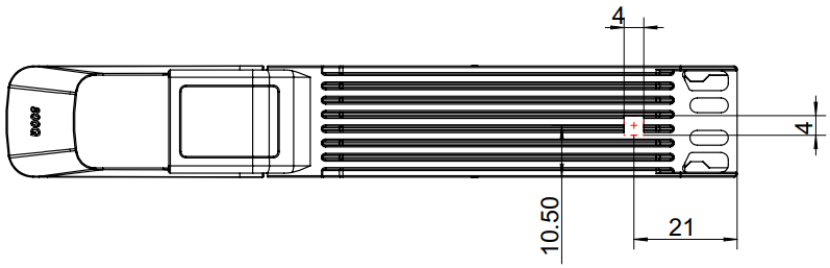


Mechanical Specifications



Case Temperature Measurement Point

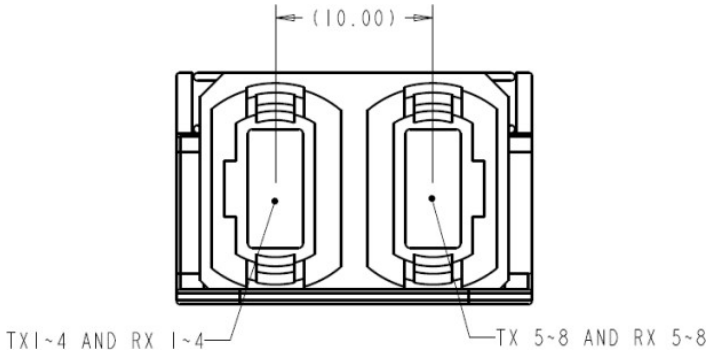
The bellow picture shows the location of the hottest spot for measuring module case temperature. In addition, the digital diagnostic monitors (DDM) temperature is also calibrated to this spot.



Notes:

1. All dimensions are in mm.

Module Optical Interface (Looking into the Optical Port)



Notes:

1. The optical interface port is a male dual MPO-12 connector as specified in IEC 61754-7-1 mates with a standard type MPO-12 female plug connector with down-angled interface.

About Us:

Proline Options is one of North America's leading providers of transceivers and high speed cabling. With a reputation for quality, tested products that cover the connectivity spectrum, Proline Options has a solution for you regardless of the specification.

At Proline Options, every product is tested in its intended application - never batch or spec tested only. We run bandwidth, distance and IOS network tests. We have documented an impressive 0.03% failure rate over the last 10 years. To continue this rate of success we invest millions annually in our own on-site testing lab.

Tel: 855.933.3223
Email: sales@prolineoptions.com
Email: techsupport@prolineoptions.com
Web: https://www.prolineoptions.com