CAB-D-4Q-400G-1M-PRO

Arista Networks® CAB-D-4Q-400G-1M Compatible TAA 400GBase-CU QSFP-DD to 4xQSFP56 Direct Attach Cable (Passive Twinax, 1m)

Features

- Compliant with QSFP-DD MSA Specification Rev 3.4
- SFF-8636 management interface support
- SFF-8679 electrical interface compliant
- Supports aggregate data rates of 100 and 400Gbps
- I2C for EEPROM communication
- Compatible with IEEE 802.3bj, IEEE 802.3by, IEEE 802.3cd
- Excellent EMI/EMC performance 360-degree cable shield termination
- Pull-to-release slide latch design
- Low loss, stronger mechanical features, more flexible
- Advantage dual side pre-solder automated assembly technologies
- RoHS Compliant and Lead-Free

Applications:

- Switches, Servers and Routers
- Data Center Networks
- Storage Area Networks
- High Performance Computing

Product Description

This is a Arista Networks® CAB-D-4Q-400G-1M Compatible 400GBase-CU QSFP-DD to 4xQSFP56 direct attach cable that operates over passive copper with a maximum reach of 1m. It has been programmed, uniquely serialized, and data-traffic and application tested to ensure it is 100% compliant and functional. We stand behind the quality of our products and proudly offer a limited lifetime warranty. This cable is TAA (Trade Agreements Act) compliant and is built to comply with MSA (Multi-Source Agreement) standards.

Proline's transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S. – made or designated country end products.

Mechanical Characteristics

Cable Jacket Material	Flammability Rating
PVC	VW-1

Electrical Characteristics

Parameter	Specification
Impedance	100Ω
Data Rate	56Gbps per lane (PAM-4)
Voltage	3.3V DC
Current (signal application only)	0.75A
Operating Temperature	-10°C to 55°C
Storage Temperature	-10°C to 55°C
High Speed Compliant	IEEE 802.3cd

QSFP-DD to 4xQSFP Wiring Schematic

P1 (QSFP-DD)			P2 (QSFP)	
GND				GND
TX1+	36	<⟷>	17	RX1+
TX1-	37	<⟷>	18	RX1-
GND				GND
TX2+	3	<⟷>	22	RX2+
TX2-	2	<⟷>	21	RX2-
GND				GND
GND				GND
RX1+	17	<⟷>	36	TX1+
RX1-	18	<⟷>	37	TX1-
GND				GND
RX2+	22	<⟷>	3	TX2+
RX2-	21	<⟷>	2	TX2-
GND				GND

P1 (QSFP-DD)			P3 (QSFP)	
GND				GND
TX3+	33	<⟷>	17	RX1+
TX3-	34	<⟷>	18	RX1-
GND				GND
TX4+	6	<⟷>	22	RX2+
TX4-	5	<⟷>	21	RX2-
GND				GND
GND				GND
RX3+	14	<⟷>	36	TX1+
RX3-	15	<⟷>	37	TX1-
GND				GND
RX4+	25	<⟷>	3	TX2+
RX4-	24	<⟷>	2	TX2-
GND				GND

P1 (QSFP-DD)			P4 (QSFP)	
GND				GND
TX5+	74	<⟷>	17	RX1+
TX5-	75	<⟷>	18	RX1-
GND				GND
TX6+	41	<⟷>	22	RX2+
TX6-	40	<⟷>	21	RX2-
GND				GND
GND				GND
RX5+	55	<⟷>	36	TX1+
RX5-	56	<⟷>	37	TX1-
GND				GND
RX6+	60	<⟷>	3	TX2+
RX6-	59	<⟷>	2	TX2-
GND				GND

P1 (QSFP-DD)			P5 (QSFP)	
GND				GND
TX7+	71	<⟷>	17	RX1+
TX7-	72	<⟷>	18	RX1-
GND				GND
TX8+	44	<⟷>	22	RX2+
TX8-	43	<⟷>	21	RX2-
GND				GND
GND				GND
RX7+	52	<⟷>	36	TX1+
RX7-	53	<⟷>	37	TX1-
GND				GND
RX8+	63	<⟷>	3	TX2+
RX8-	62	<⟷>	2	TX2-
GND				GND

QSFP-DD Pin Descriptions

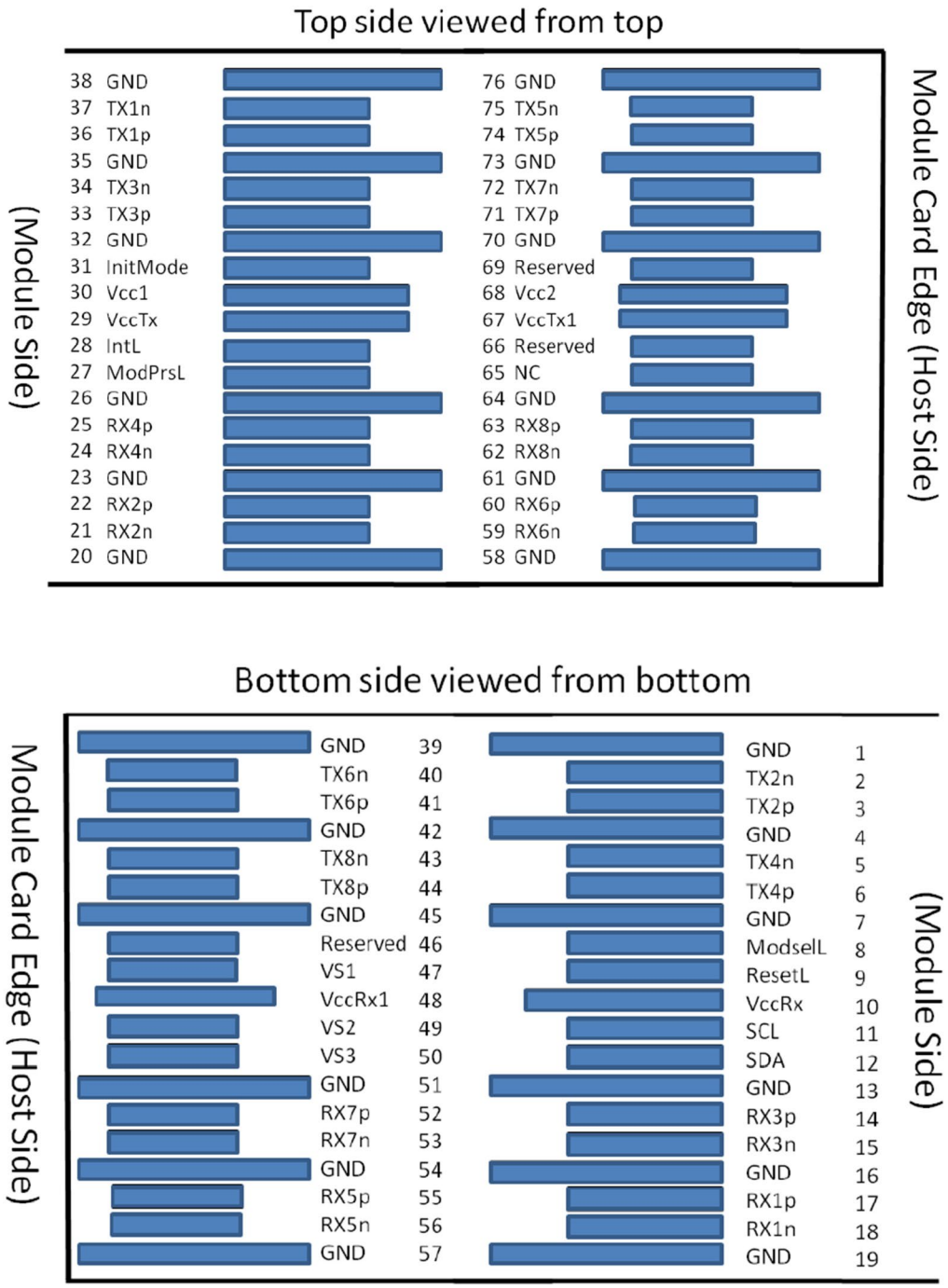
PIN	Logic	Symbol	Description	Notes
1		GND	Ground.	1
2	CML-I	Tx2-	Transmitter Inverted Data Input.	
3	CML-I	Tx2+	Transmitter Non-Inverted Data Input.	
4		GND	Ground.	1
5	CML-I	Tx4-	Transmitter Inverted Data Input.	
6	CML-I	Tx4+	Transmitter Non-Inverted Data Input.	
7		GND	Ground.	1
8	LVTTL-I	ModSelL	Module Select.	
9	LVTTL-I	ResetL	Module Reset.	
10		VccRx	+3.3V Power Supply Receiver.	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock.	
12	LVCMOS-I/O	SDA	2-wire serial interface data.	
13		GND	Ground.	1
14	CML-O	Rx3+	Receiver Non-Inverted Data Output.	
15	CML-O	Rx3-	Receiver Inverted Data Output.	
16		GND	Ground.	1
17	CML-O	Rx1+	Receiver Non-Inverted Data Output.	
18	CML-O	Rx1-	Receiver Inverted Data Output.	
19		GND	Ground.	1
20		GND	Ground.	1
21	CML-O	Rx2-	Receiver Inverted Data Output.	
22	CML-O	Rx2+	Receiver Non-Inverted Data Output.	
23		GND	Ground.	1
24	CML-O	Rx4-	Receiver Inverted Data Output.	
25	CML-O	Rx4+	Receiver Non-Inverted Data Output.	
26		GND	Ground.	1
27	LVTTL-O	ModPrsL	Module Present.	
28	LVTTL-O	IntL	Interrupt.	
29		VccTx	+3.3V Power Supply Transmitter.	2
30		Vccl	+3.3V Power Supply.	2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE.	
32		GND	Ground.	1
33	CML-I	Tx3+	Transmitter Non-Inverted Data Input.	
34	CML-I	Tx3-	Transmitter Inverted Data Input.	
35		GND	Ground.	1
36	CML-I	Tx1+	Transmitter Non-Inverted Data Input.	
37	CML-I	Tx1-	Transmitter Inverted Data Input.	
38		GND	Ground.	1

PIN		Symbol	Description	Notes
39		GND	Ground.	1
40	CML-I	Tx6-	Transmitter Inverted Data Input.	
41	CML-I	Tx6+	Transmitter Non-Inverted Data Input.	
42		GND	Ground.	1
43	CML-I	Tx8-	Transmitter Inverted Data Input.	
44	CML-I	Tx8+	Transmitter Non-Inverted Data Input.	
45		GND	Ground.	1
46		Reserved	For future use.	3
47		VSl	Module Vendor Specific 1.	3
48		VccRx1	3.3V Power Supply.	2
49		VS2	Module Vendor Specific 2.	3
50		VS3	Module Vendor Specific 3.	3
51		GND	Ground.	1
52	CML-O	Rx7+	Receiver Non-Inverted Data Output.	
53	CML-O	Rx7-	Receiver Inverted Data Output.	
54		GND	Ground.	1
55	CML-O	Rx5+	Receiver Non-Inverted Data Output.	
56	CML-O	Rx5-	Receiver Inverted Data Output.	
57		GND	Ground.	1
58		GND	Ground.	1
59	CML-O	Rx6-	Receiver Inverted Data Output.	
60	CML-O	Rx6+	Receiver Non-Inverted Data Output.	
61		GND	Ground.	1
62	CML-O	Rx8-	Receiver Inverted Data Output.	
63	CML-O	Rx8+	Receiver Non-Inverted Data Output.	
64		GND	Ground.	1
65		NC	No Connect.	3
66		Reserved	For future use.	3
67		VccTx1	3.3V Power Supply.	2
68		Vcc2	3.3V Power Supply.	2
69		Reserved	For future use.	3
70		GND	Ground.	1
71	CML-I	Tx7+	Transmitter Non-Inverted Data Input.	
72	CML-I	Tx7-	Transmitter Inverted Data Input.	
73		GND	Ground.	1
74	CML-I	Tx5+	Transmitter Non-Inverted Data Input.	
75	CML-I	Tx5-	Transmitter Inverted Data Input.	
76		GND	Ground.	1

Notes:

1. QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A,3B.

QSFP-DD Electrical Pin-out Details



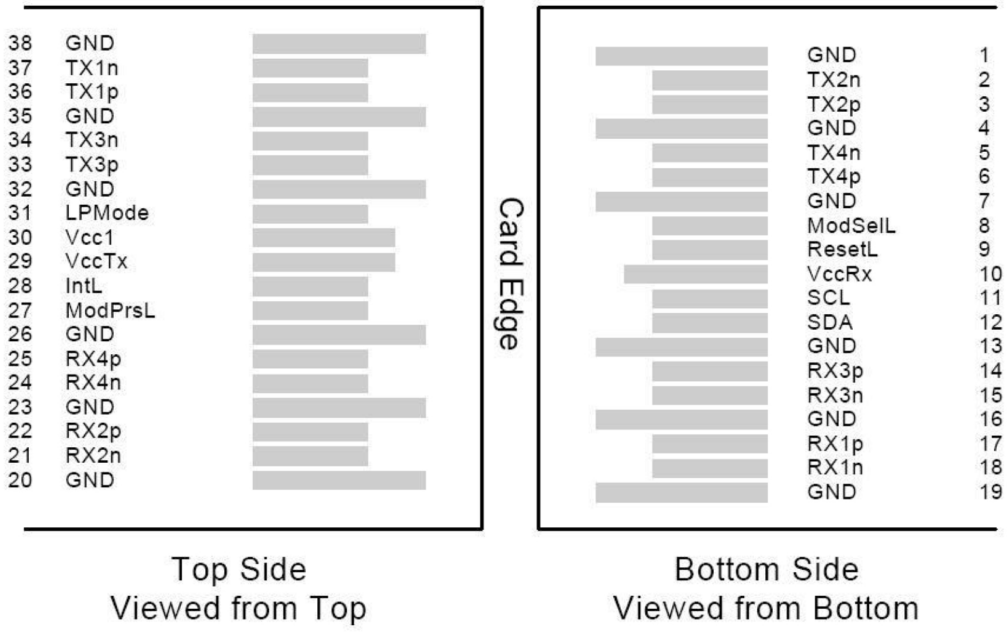
QSFP56 Pin Definitions

Pin	Logic	Symbol	Name/Descriptions	Ref.
1		GND	Module Ground.	1
2	CML-I	Tx2-	Transmitter inverted data input.	
3	CML-I	Tx2+	Transmitter non-inverted data input.	
4		GND	Module Ground.	1
5	CML-I	Tx4-	Transmitter inverted data input.	
6	CML-I	Tx4+	Transmitter non-inverted data input.	
7		GND	Module Ground.	1
8	LVTTL-I	MODSEIL	Module Select.	2
9	LVTTL-I	ResetL	Module Reset.	2
10		VCCRx	+3.3v Receiver Power Supply.	
11	LVCMOS-I	SCL	2-wire Serial interface clock.	2
12	LVCMOS-I/O	SDA	2-wire Serial interface data.	2
13		GND	Module Ground.	1
14	CML-O	RX3+	Receiver non-inverted data output.	
15	CML-O	RX3-	Receiver inverted data output.	
16		GND	Module Ground.	1
17	CML-O	RX1+	Receiver non-inverted data output.	
18	CML-O	RX1-	Receiver inverted data output.	
19		GND	Module Ground.	1
20		GND	Module Ground.	1
21	CML-O	RX2-	Receiver inverted data output.	
22	CML-O	RX2+	Receiver non-inverted data output.	
23		GND	Module Ground.	1
24	CML-O	RX4-	Receiver inverted data output.	
25	CML-O	RX4+	Receiver non-inverted data output.	
26		GND	Module Ground.	1
27	LVTTL-O	ModPrsL	Module Present, internal pulled down to GND.	
28	LVTTL-O	IntL	Interrupt output should be pulled up on host board.	2
29		VCCTx	+3.3v Transmitter Power Supply.	
30		VCC1	+3.3v Power Supply.	
31	LVTTL-I	LPMode	Low Power Mode.	2
32		GND	Module Ground.	1
33	CML-I	Tx3+	Transmitter non-inverted data input.	
34	CML-I	Tx3-	Transmitter inverted data input.	
35		GND	Module Ground.	1
36	CML-I	Tx1+	Transmitter non-inverted data input.	
37	CML-I	Tx1-	Transmitter inverted data input.	
38		GND	Module Ground.	1

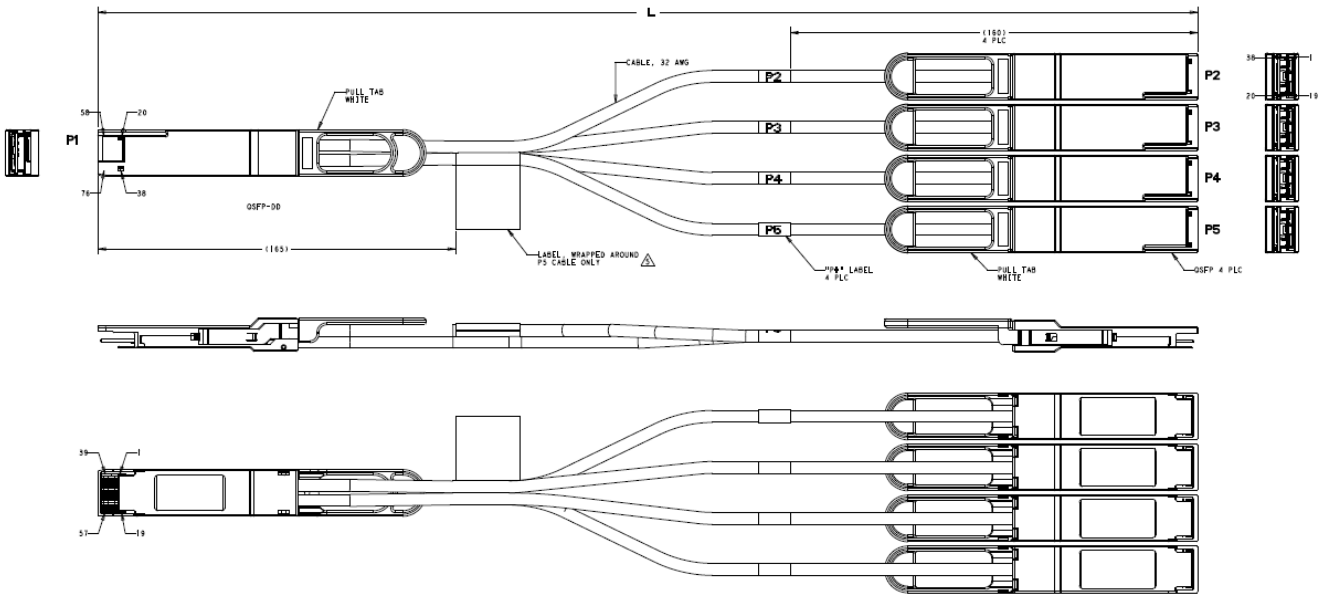
Notes:

1. Module circuit ground is isolated from module chassis ground with in the module.
2. Open collector; should be pulled up with 4.7k-10k ohms on host board to a voltage between 3.15V and 3.6V.

QSFP56 Electrical Pin-out Details



Mechanical Specifications



About Us:

Proline Options is one of North America's leading providers of transceivers and high speed cabling. With a reputation for quality, tested products that cover the connectivity spectrum, Proline Options has a solution for you regardless of the specification.

At Proline Options, every product is tested in its intended application - never batch or spec tested only. We run bandwidth, distance and IOS network tests. We have documented an impressive 0.03% failure rate over the last 10 years. To continue this rate of success we invest millions annually in our own on-site testing lab.

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