

40GB-LR4-QSFP-PRO

Enterasys® 40GB-LR4-QSFP Compatible TAA Compliant 40GBase-LR4 QSFP+ Transceiver (SMF, 1270nm to 1330nm, 10km, DOM, 0 to 70C, LC)

Features

- SFF-8436 Compliance
- Duplex LC Connector
- Commercial Temperature 0 to 70 Celsius
- Single-mode Fiber
- Hot Pluggable
- Excellent ESD Protection
- Metal with Lower EMI
- RoHS Compliant and Lead Free



Applications:

- 40GBase Ethernet
- Access and Enterprise

Product Description

This Enterasys® 40GB-LR4-QSFP compatible QSFP+ transceiver provides 40GBase-LR4 throughput up to 10km over single-mode fiber (SMF) using a wavelength of 1270nm to 1330nm via an LC connector. It is guaranteed to be 100% compatible with the equivalent Enterasys® transceiver. This easy to install, hot swappable transceiver has been programmed, uniquely serialized and data-traffic and application tested to ensure that it will initialize and perform identically. Digital optical monitoring (DOM) support is also present to allow access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

Proline's transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S. – made or designated country end products.



Absolute Maximum Ratings

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|----------------------------|--------|------|------|------|------|
| Storage Temperature | TS | -40 | | 85 | °C |
| Relative Humidity | Rh | 0 | | 85 | % |
| Supply Voltage | Vcc | -0.5 | | 4.0 | V |
| Case Operating Temperature | Tc | 0 | | 70 | °C |

Electrical Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Notes |
|--|----------------------------|------|------|------|--------|--------------------------------|
| Power Supply Voltage | Vcc | 3.13 | 3.3 | 3.47 | V | |
| Power Consumption | | | | 3.5 | W | |
| Supply Current | ICC | | 0.75 | 1.0 | A | |
| Control I/O Voltage, High | VIH | 2.0 | | VCC | V | |
| Control I/O Voltage, Low | VIL | 0 | | 0.7 | V | |
| Inter-Channel Skew | TSK | | | 150 | ps | |
| RESETL Duration | | | 10 | | us | |
| RESETL De-assert time | | | | 100 | ms | |
| Power on time | | | | 100 | ms | |
| Transmitter | | | | | | |
| Single Ended Output Voltage Tolerance | | -0.3 | | 4 | V | |
| AC Common mode Voltage Tolerance (RMS) | | 15 | | | mV | |
| Tx Input Diff Voltage | VI | 90 | | 1600 | mV | |
| Tx Input Diff Impedance | ZIN | 80 | 100 | 120 | Ω | |
| Differential Input Return Loss | See IEEE 802.3ba 86A.4.11 | | | | dB | 10MHz-11.1GHz |
| J2 Jitter tolerance | Jt2 | | | 0.18 | UI | |
| J9 Jitter Tolerance | Jt9 | | | 0.26 | UI | |
| Data Dependent Pulse Width Shrinkage | DDPWS | | | 0.07 | UI | |
| Eye Mask Coordinates: X1, X2, Y1, Y2 | 0.1, 0.31, 95, 350 | | | | | |
| Receiver | | | | | | |
| Single Ended Output Voltage Tolerance | | -0.3 | | 4 | V | Preferred to TP1 signal common |
| AC Common mode Voltage Tolerance (RMS) | | | | 7.5 | mV | |
| Termination Mismatch at 1MHz | | | | 5 | % | |
| Differential Output Return Loss | See IEEE 802.3ba 86A.4.2.1 | | | | dB | 10MHz-11.1GHz |
| Common-mode Output Return Loss | See IEEE 802.3ba 86A.4.2.1 | | | | dB | 10MHz-11.1GHz |
| Rx Output Diff Voltage | Vo | | 600 | 800 | mV | |
| Rx Output Rise and Fall Time | Tr/Tf | | | 35 | ps | 20% to 80% |
| J2 Jitter Tolerance | Jr2 | | | 0.46 | UI | |
| J9 Jitter Tolerance | Jr9 | | | 0.63 | UI | |
| Eye Mask Coordinates: X1, X2, Y1, Y2 | 0.29, 0.5, 150, 425 | | | | UI, mV | |

Notes:

1. The single ended input voltage tolerance is the allowable range of the instantaneous input signals

Optical Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Notes |
|---|--|--------|------|--------|-------|-----------------|
| Wavelength | L0 | 1264.5 | 1271 | 1277.5 | nm | |
| | L1 | 1284.5 | 1291 | 1297.5 | nm | |
| | L2 | 1304.5 | 1311 | 1317.5 | nm | |
| | L3 | 1324.5 | 1331 | 1337.5 | nm | |
| Transmitter | | | | | | |
| Side-mode Suppression Ratio | SMSR | 30 | | | dB | |
| Total Average Launch Power | P_T | | | 8.3 | dBm | |
| Average Launch Power, each Lane | | -7 | | 2.3 | dBm | |
| Optical Modulation Amplitude, each Lane | OMA | -4 | | 3.5 | dBm | |
| Difference in launch Power between any two lanes (OMA) | | | | 6.5 | dB | |
| Launch Power in OMA minus Transmitter and Dispersion Penalty (TDP), each Lane | | -4.8 | | | dBm | |
| TDP, each Lane | TDP | | | 2.3 | dB | |
| Extinction Ratio | ER | 3.5 | | | dB | |
| Relative Intensity Noise | R_{in} | | | -128 | dB/Hz | 12dB reflection |
| Optical Return Loss Tolerance | | | | 20 | dB | |
| Transmitter Reflectance | R_T | | | -12 | dB | |
| Transmitter Eye Mask Definition X1, X2, X3, Y1, Y2, Y3 | Specification Values 0.25, 0.4, 0.45, 0.25, 0.28, 0.4 | | | | | |
| Average Launch Power OFF Transmitter, each Lane | P_{off} | | | -30 | dBm | |
| Receiver | | | | | | |
| Damage Threshold | TH_d | 3.3 | | | dBm | 1 |
| Average Power at receiver Input, each Lane | | -13.7 | | 2.3 | dB | |
| Receiver Reflectance | R_R | | | -26 | dB | |
| Receiver Power (OMA), each Lane | | | | 3.5 | dBm | |
| Stressed Receiver Sensitivity in OMA, each Lane | | | | -9.9 | dBm | |
| Receiver Sensitivity, each Lane | S_R | | | -11.5 | dBm | |
| Difference in Receive Power between any Lanes (OMA) | | | | -7.5 | dBm | |
| Condition of Stress Receiver Sensitivity Test | | | | | | |
| Vertical Eye Closure Penalty, each Lane | | | 1.6 | | dB | |
| Stressed Eye Jitter, each Lane | | | 0.3 | | UI | |

Notes:

1. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.

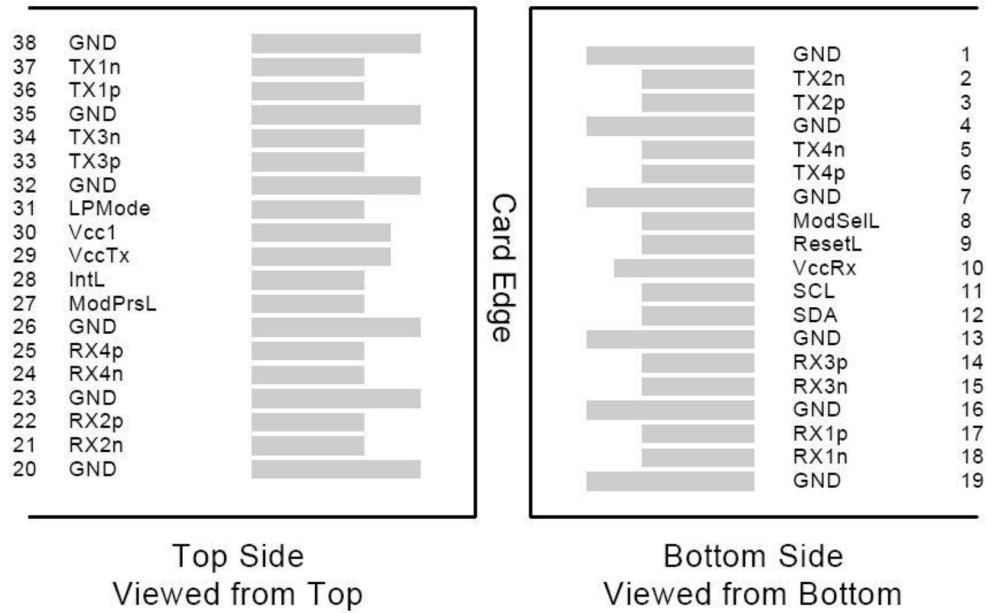
Pin Descriptions

| Pin | Logic | Symbol | Name/Descriptions | Ref. |
|-----|-------------|---------|--|------|
| 1 | | GND | Module Ground | 1 |
| 2 | CML-I | Tx2- | Transmitter inverted data input | |
| 3 | CML-I | Tx2+ | Transmitter non-inverted data input | |
| 4 | | GND | Module Ground | 1 |
| 5 | CML-I | Tx4- | Transmitter inverted data input | |
| 6 | CML-I | Tx4+ | Transmitter non-inverted data input | |
| 7 | | GND | Module Ground | 1 |
| 8 | LVTTTL-I | MODSEIL | Module Select | 2 |
| 9 | LVTTTL-I | ResetL | Module Reset | 2 |
| 10 | | VCCRx | +3.3v Receiver Power Supply | |
| 11 | LVC MOS-I | SCL | 2-wire Serial interface clock | 2 |
| 12 | LVC MOS-I/O | SDA | 2-wire Serial interface data | 2 |
| 13 | | GND | Module Ground | 1 |
| 14 | CML-O | RX3+ | Receiver non-inverted data output | |
| 15 | CML-O | RX3- | Receiver inverted data output | |
| 16 | | GND | Module Ground | 1 |
| 17 | CML-O | RX1+ | Receiver non-inverted data output | |
| 18 | CML-O | RX1- | Receiver inverted data output | |
| 19 | | GND | Module Ground | 1 |
| 20 | | GND | Module Ground | 1 |
| 21 | CML-O | RX2- | Receiver inverted data output | |
| 22 | CML-O | RX2+ | Receiver non-inverted data output | |
| 23 | | GND | Module Ground | 1 |
| 24 | CML-O | RX4- | Receiver inverted data output | |
| 25 | CML-O | RX4+ | Receiver non-inverted data output | |
| 26 | | GND | Module Ground | 1 |
| 27 | LVTTTL-O | ModPrsL | Module Present, internal pulled down to GND | |
| 28 | LVTTTL-O | IntL | Interrupt output should be pulled up on host board | 2 |
| 29 | | VCCTx | +3.3v Transmitter Power Supply | |
| 30 | | VCC1 | +3.3v Power Supply | |
| 31 | LVTTTL-I | LPMode | Low Power Mode | 2 |
| 32 | | GND | Module Ground | 1 |
| 33 | CML-I | Tx3+ | Transmitter non-inverted data input | |
| 34 | CML-I | Tx3- | Transmitter inverted data input | |
| 35 | | GND | Module Ground | 1 |
| 36 | CML-I | Tx1+ | Transmitter non-inverted data input | |
| 37 | CML-I | Tx1- | Transmitter inverted data input | |
| 38 | | GND | Module Ground | 1 |

Notes:

1. Module circuit ground is isolated from module chassis ground with in the module.
2. Open collector; should be pulled up with 4.7k-10k ohms on host board to a voltage between 3.15V and 3.6V.

Electrical Pin-out Details

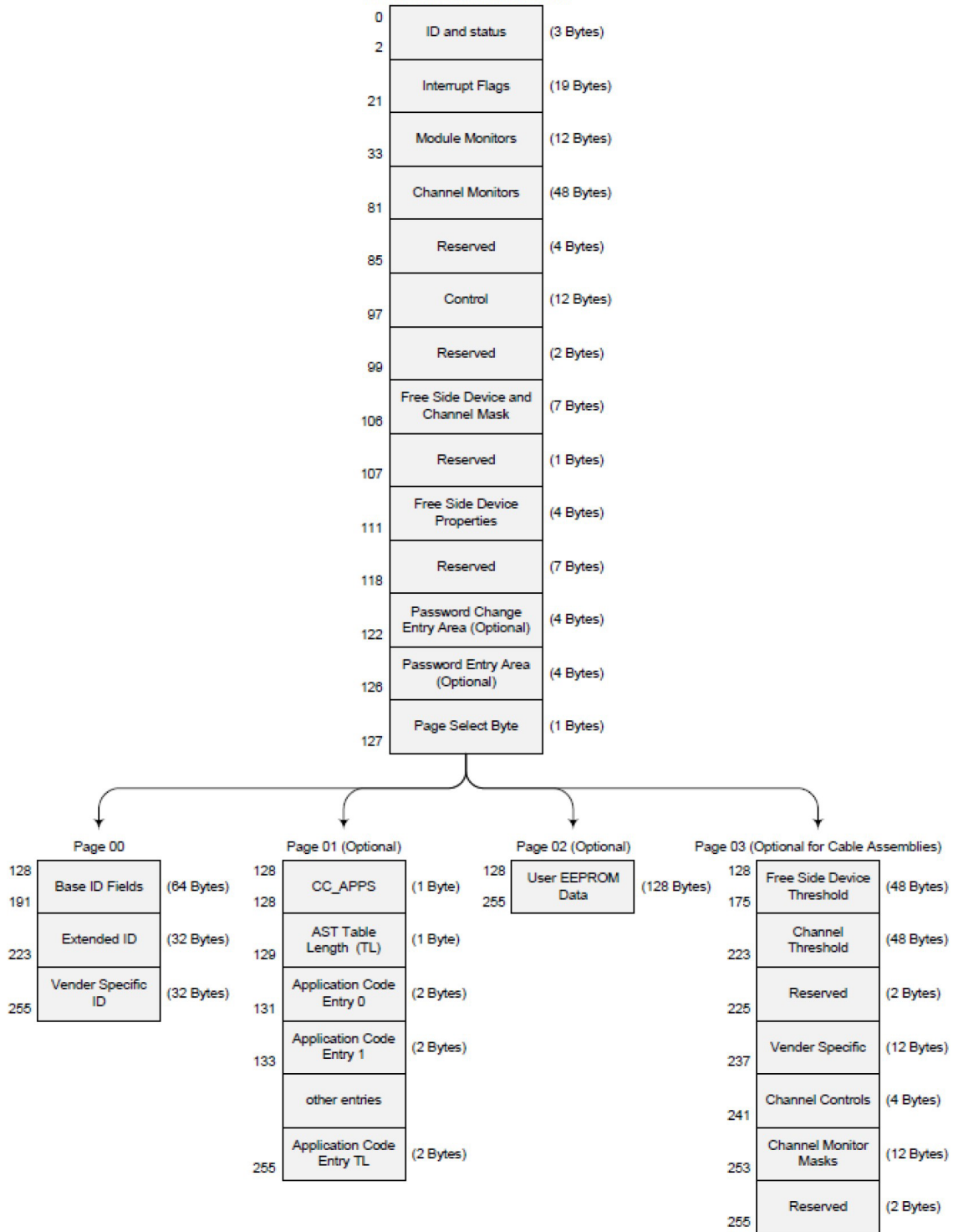


Recommended Circuit Schematic

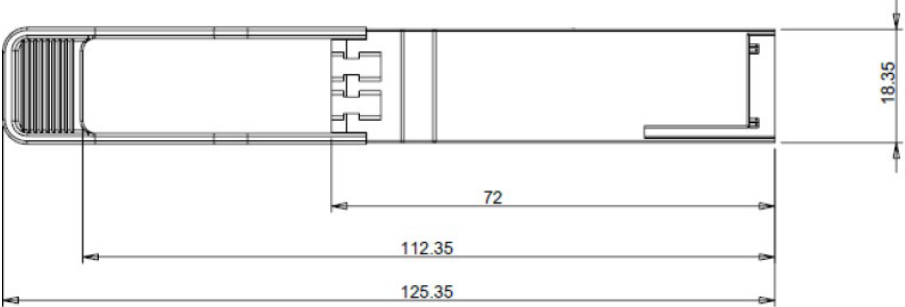
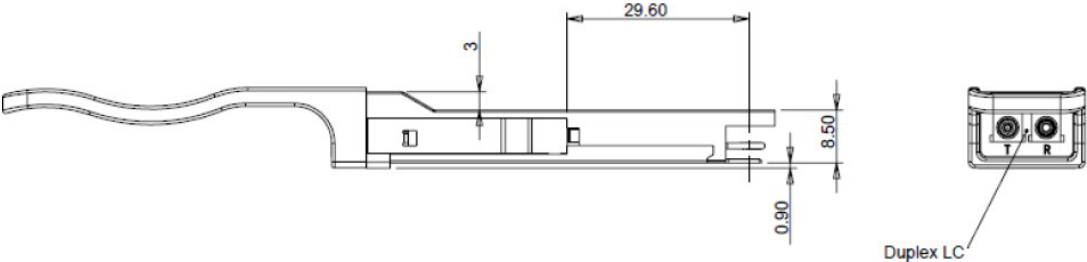


EEPROM Information

2-Wire Serial Address: 1010000x



Mechanical Specifications



About Us:

Proline Options is one of North America's leading providers of transceivers and high speed cabling. With a reputation for quality, tested products that cover the connectivity spectrum, Proline Options has a solution for you regardless of the specification.

At Proline Options, every product is tested in its intended application - never batch or spec tested only. We run bandwidth, distance and IOS network tests. We have documented an impressive 0.03% failure rate over the last 10 years. To continue this rate of success we invest millions annually in our own on-site testing lab.



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