

### 34060727-PRO

Huawei® 34060727 Compatible TAA Compliant 100GBase-LR4 CFP2 Transceiver (SMF, 1310nm, 10km, DOM, 0 to 70C, LC)

#### Features

- CFP MSA 1.0 Compliance
- Duplex LC Connector
- Commercial Temperature 0 to 70 Celsius
- Single-mode Fiber
- Hot Pluggable
- Excellent ESD Protection
- Metal with Lower EMI
- RoHS Compliant and Lead Free



#### Applications:

- 100GBase Ethernet
- OTU4 Operation
- Access and Enterprise

#### Product Description

This Huawei® 34060727 compatible CFP2 transceiver provides 100GBase-LR4 throughput up to 10km over single-mode fiber (SMF) using a wavelength of 1310nm via an LC connector. It is guaranteed to be 100% compatible with the equivalent Huawei® transceiver. This easy to install, hot swappable transceiver has been programmed, uniquely serialized and data-traffic and application tested to ensure that it will initialize and perform identically. Digital optical monitoring (DOM) support is also present to allow access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

Proline's transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S. – made or designated country end products.



## Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Notes
Storage Temperature	TS	-40	+85	°C	
Power Supply Voltage	VCC	-0.5	3.6	V	
Operating Case Temperature Range	Tc	0	+70	°C	
Relative Humidity	Rh	5	85	%	
ESD			500	V	2

### Notes:

1. Exceeding any one of these values may destroy the device immediately.
2. Human body model.

## Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage	VCC	3.2	3.3	3.4	V	
Power Consumption	P			6	W	
<b>Transmitter</b>						
Differential Input Amplitude	Vin			900	mVpp	AC coupled inputs
Input differential impedance	Zin	80	100	115	Ω	Rin > 100kohms @ DC
<b>Receiver</b>						
Differential output amplitude	Vout			900	mVpp	AC coupled outputs
Output differential impedance	Zoout	80	100	120	Ω	

## 1.2V MDIO Interface Specifications

Parameter	Symbol	Min.	Typ.	Max	Unit	Notes
Input Voltage	V <sub>IH</sub>	0.84		1.5	V	
	V <sub>IL</sub>	-0.3		0.36	V	
Input Leak current	I <sub>IN</sub>	-100		100	uA	
Output Voltage	V <sub>OH</sub>	1.0		1.5	V	
	V <sub>OL</sub>	-0.3		0.2	V	
Input Capacitance	C <sub>I</sub>			10	pF	
Input MDC Clock	f <sub>MDC</sub>	0.1		4	MHz	
MDC Clock Period	T <sub>MDC</sub>	250		10000	ns	
MDIO Hold Time	T <sub>hold</sub>	10			ns	
MDIO Setup Time	T <sub>setup</sub>	10			ns	
Clock to output delay from the MMD	T <sub>dely</sub>	0		300	ns	
GLB_ALM	T <sub>glb_alm_ass</sub>			150	ms	
	T <sub>glb_alm_dea</sub>			150	ms	
MDC High time	T <sub>high</sub>			160	ns	
MDC Low time	T <sub>low</sub>			160	ns	

## OTU4 Operation Optical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
<b>Transmitter</b>						
Signaling Speed per Lane	BRAVE		27.95		Gbps	
Data Rate Variation		-20		+20		
Lane_0 Center Wavelength	$\lambda_{C0}$	1294.53	1295.56	1296.59	nm	
Lane_1 Center Wavelength	$\lambda_{C1}$	1299.02	1300.05	1301.09	nm	
Lane_2 Center Wavelength	$\lambda_{C2}$	1303.54	1304.58	1305.63	nm	
Lane_3 Center Wavelength	$\lambda_{C3}$	1308.09	1309.14	1310.19	nm	
Total Average Output Power	PO1			8.9	dBm	1, 2
Average Launch Power per Lane	Peach1	-2.5		2.9	dBm	2
Maximum channel power difference				5	dB	
Side Mode Suppression Ratio	SMSR	30			dB	
Optical Return Loss Tolerance				20	dB	2
Extinction Ratio	ER1	7			dB	
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}		G.959.1 Compliant				2
Optical Eye Mask Margin	MM	5			%	3
TX Disable Assert Time	t_off			100	us	
<b>Receiver</b>						
Signaling Speed per Lane	BRAVE		27.95		Gbps	
Data Rate Variation		-20		+20	ppm	
Lane_0 Center Wavelength	$\lambda_{C0}$	1294.53	1295.56	1296.59	nm	
Lane_1 Center Wavelength	$\lambda_{C1}$	1299.02	1300.05	1301.09	nm	
Lane_2 Center Wavelength	$\lambda_{C2}$	1303.54	1304.58	1305.63	nm	
Lane_3 Center Wavelength	$\lambda_{C3}$	1308.09	1309.14	1310.19	nm	
Average Receive Power per Lane	Rpow1	-8.8		2.9	dBm	4
Equivalent Sensitivity per Lane	Pmin1			-10.3	dBm	5
Damage Threshold per Lane	Pmax	5.5			dBm	
Maximum channel power difference				5.5	dB	
Maximum optical path penalty				1.5	dB	
Optical Return Loss	ORL			-26	dB	
LOS Assert	LOSA	-21	-17	-16	dBm	
LOS De-Assert	LOSD		-16	-15	dBm	
LOS Hysteresis		0.5			dB	

**Notes:**

1. Output is coupled into a 9/125µm single-mode fiber.
2. Filtered, measured with a PRBS 2<sup>31</sup>-1 test pattern @27.95Gbps
3. Eye Margin within 1000 waveforms.
4. CFP2 transceiver works in OTU4 411-9D1F mode.
5. Minimum average optical power measured at BER less than 1E-12, with a 2<sup>31</sup>-1 PRBS@27.95Gbps.

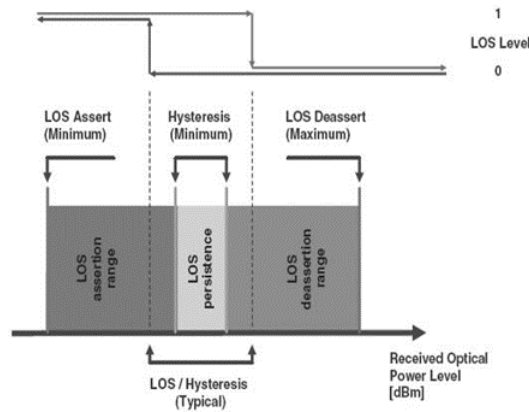
**100GBASE-LR4 Operation Optical Characteristics**

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes	
<b>Transmitter</b>							
Signaling Speed per Lane	BRAVE		25.78		Gbps		
Data Rate Variation		-100		+100	ppm		
Lane_0 Center Wavelength	λC0	1294.53	1295.56	1296.59	nm		
Lane_1 Center Wavelength	λC1	1299.02	1300.05	1301.09	nm		
Lane_2 Center Wavelength	λC2	1303.54	1304.58	1305.63	nm		
Lane_3 Center Wavelength	λC3	1308.09	1309.14	1310.19	nm		
Total Average Output Power	PO2	-		10.5	dBm	1, 2	
Average Launch Power per Lane	Peach2	-4.3		4.5	dBm	2	
Side Mode Suppression Ratio	SMSR	30			dB		
Difference in launch power between any two lanes				5	dB		
Average launch power of OFF transmitter per lane				-30	dBm		
Optical Return Loss Tolerance				20	dB		
Transmitter reflectance				-12	dB		
Extinction Ratio	ER	4			dB	2	
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}		IEEE802.3ba-2010 Compliant					2
Optical Eye Mask Margin	MM	5			%	3	
TX Disable Assert Time	t_off			100	us		
<b>Receiver</b>							
Signaling Speed per Lane	BRAVE		25.78		Gbps		
Data Rate Variation		-100		+100	ppm		
Lane_0 Center Wavelength	λC0	1294.53	1295.56	1296.59	nm		
Lane_1 Center Wavelength	λC1	1299.02	1300.05	1301.09	nm		
Lane_2 Center Wavelength	λC2	1303.54	1304.58	1305.63	nm		
Lane_3 Center Wavelength	λC3	1308.09	1309.14	1310.19	nm		
Average Receive Power per Lane	Rpow2	-10.6		4.5	dBm	4	
Receive Sensitivity (OMA) per lane	Pmin2			-8.6	dBm	5	

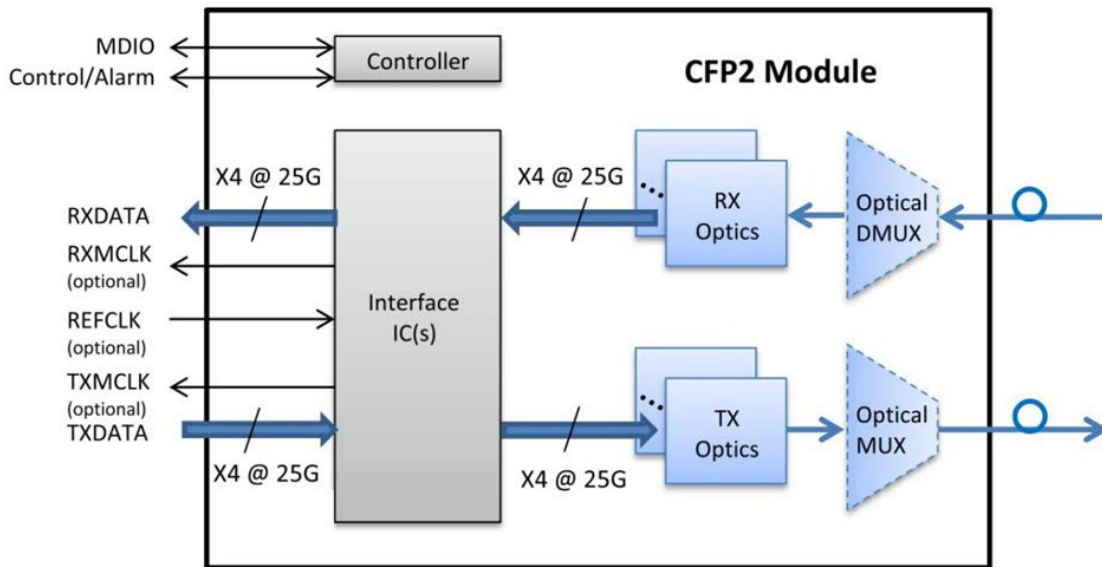
<b>Stressed Sensitivity (OMA) per lane</b>	SRS			-6.8	dBm	
<b>Damage Threshold per Lane</b>	Pmax	5.5			dBm	
<b>Optical Return Loss</b>	ORL			-26	dB	
<b>LOS Assert</b>	LOSA	-21	-17	-16	dBm	
<b>LOS De-Assert</b>	LOSD		-16	-15	dBm	
<b>LOS Hysteresis</b>		0.5			dB	6

**Notes:**

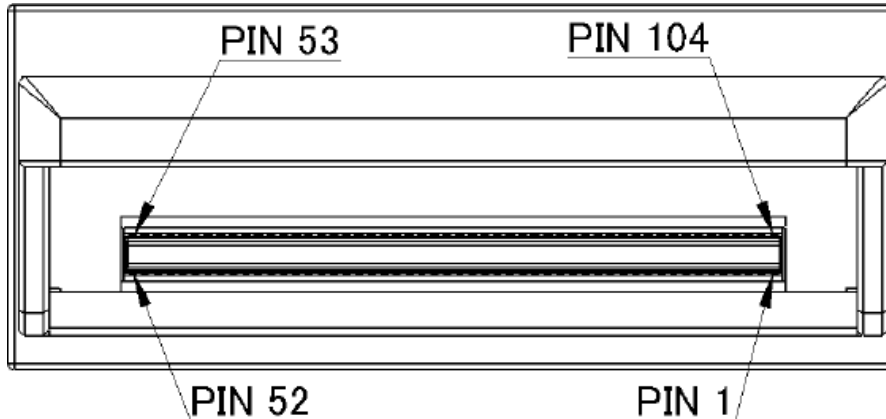
1. Output is coupled into a 9/125µm single-mode fiber.
2. Filtered, measured with a PRBS 2<sup>31</sup>-1 test pattern @25.78Gbps
3. Eye Margin within 1000 waveforms.
4. CFP2 transceiver works in 100GBASE-LR4 mode
5. Minimum average optical power measured at BER less than 1E-12, with a 2<sup>31</sup>-1 PRBS@25.78Gbps.
6. LOS Hysteresis



**Functional Description of Transceiver**



## Electrical Pad Layout



## Pin Descriptions

### Part A: Bottom Row Pin Function Definition

Pin	Name	Function	Notes
1	GND		
2	(TX_MCK_N)	O CML	For optical waveform testing. Not for normal use.
3	(TX_MCK_P)	O CML	For optical waveform testing. Not for normal use.
4	GND		
5	N.C.		
6	N.C.		
7	3.3V_GND		
8	3.3V_GND		
9	3.3V		3.3V Module Supply Voltage
10	3.3V		3.3V Module Supply Voltage
11	3.3V		3.3V Module Supply Voltage
12	3.3V		3.3V Module Supply Voltage
13	3.3V_GND		
14	3.3V_GND		
15	VND_IO_A		Module Vendor I/O A. Do not connect!
16	VND_IO_B		Module Vendor I/O B. Do not connect!
17	PRG_CNTL1		Programmable control 1 set over MDIO, MSA default: TRXIC_RSTn. TX&RX ICs reset. "0": reset; "1" or NC: enabled = not used
18	PRG_CNTL2		Programmable Control 2 set over MDIO, MSA Default: Hardware Interlock LSB, "00": ≤3W, "01": ≤6W, "10": ≤9W, "11" or NC: ≤12W = not used
19	PRG_CNTL3		Programmable Control 3 set over MDIO, MSA Default: Hardware Interlock MSB, "00": ≤3W, "01": ≤6W, "10": ≤9W, "11" or NC: ≤12W = not used
20	PRG_ALARM1		Programmable alarm 1 set over MDIO, MSA default: HIPWR_ON. "1": module power up completed; "0": module not high powered up.
21	PRG_ALARM2		Programmable alarm 2 set over MDIO, MSA default: MOD_READY. "1": ready; "0": not ready.
22	PRG_ALARM3		Programmable alarm 3 set over MDIO, MSA default: MOD_FAULT, fault detected. "1": fault; "0": not fault.
23	GND		
24	TX_DIS	I LVCMOS	Transmitter disable for all lanes. "1" or NC: transmitter disabled; "0": transmitter enabled.

25	RX_LOS	O LVCMOS	Receiver loss of optical signal. "1": low optical signal; "0": normal condition.
26	MOD_LOPWR	I LVCMOS	Module Low power mode. "1" or NC: module in low power (safe) mode; "0": power-on enabled.
27	MOD_ABS	O GND	Module Absent. "1" or NC: module absent; "0": module present. Pull up resistor on Host.
28	MOD_RSTn	I LVCMOS	Module Reset. "0": resets the module; "1" or NC: module enabled. Pull Down Resistor in module.
29	GLB_ALRMn	O LVCMOS	Global Alarm. "0": alarm condition in any MDIO alarm register; "1": no alarm condition. Open Drain, Pull up resistor on Host
30	GND		
31	MDC	I 1.2V CMOS	Management Data Clock
32	MDIO	I/O 1.2V CMOS	Management Data I/O bi-directional data
33	PRTADR0	I 1.2V CMOS	MDIO Physical Port address bit 0
34	PRTADR1	I 1.2V CMOS	MDIO Physical Port address bit 1
35	PRTADR2	I 1.2V CMOS	MDIO Physical Port address bit 2
36	VND_IO_C	I/O	Module Vendor I/O C. Do not connect!
37	VND_IO_D	I/O	Module Vendor I/O D. Do not connect!
38	VND_IO_E	I/O	Module Vendor I/O E. Do not connect!
39	3.3V_GND		
40	3.3V_GND		
41	3.3V		3.3V Module Supply Voltage
42	3.3V		3.3V Module Supply Voltage
43	3.3V		3.3V Module Supply Voltage
44	3.3V		3.3V Module Supply Voltage
45	3.3V_GND		
46	3.3V_GND		
47	N.C.		No Connect
48	N.C.		No Connect
49	GND		
50	(RX_MCK_N)	O CML	For optical waveform testing. Not for normal use.
51	(RX_MCK_P)	O CML	For optical waveform testing. Not for normal use.
52	GND		

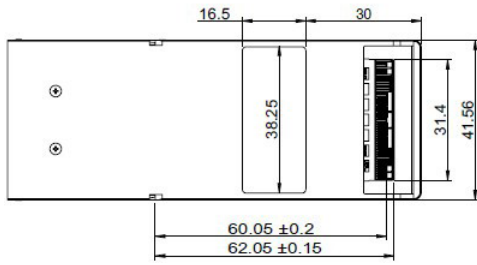
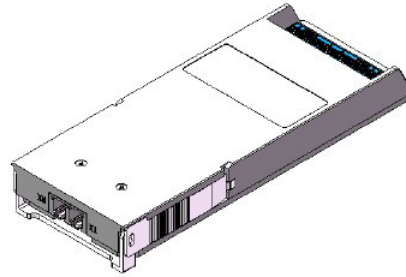
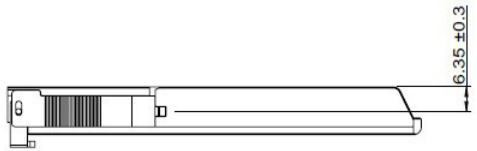
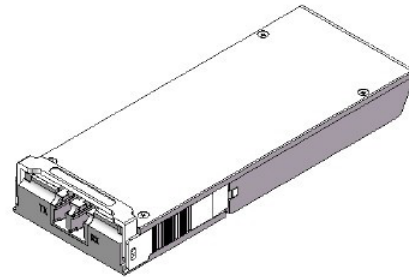
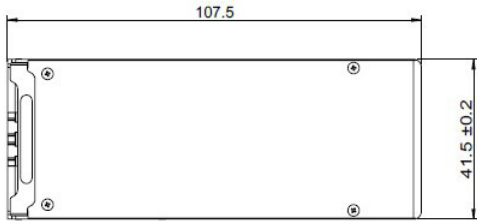
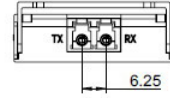
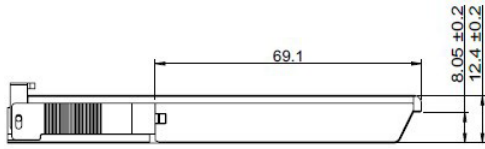
#### Part B: Top Row Pin Function Definition

Pin	Name	Function	Notes
53	GND		
54	N.C.		
55	N.C.		
56	GND		
57	RX0p	Lane 0 Rx Output O	CML Output
58	RX0n	Lane 0 Rx Output O	CML Output
59	GND		
60	RX1p	Lane 1 Rx Output O	CML Output
61	RX1n	Lane 1 Rx Output O	CML Output
62	GND		
63	N.C.		
64	N.C.		



65	GND		
66	N.C.		
67	N.C.		
68	GND		
69	RX2p	Lane 2 Rx Output O	CML Output
70	RX2n	Lane 2 Rx Output O	CML Output
71	GND		
72	RX3p	Lane 3 Rx Output O	CML Output
73	RX3n	Lane 3 Rx Output O	CML Output
74	GND		
75	N.C.		
76	N.C.		
77	GND		
78	(REFCLKn)	Reference Clock I	Reference Clock Input
79	(REFCLKp)	Reference Clock I	Reference Clock Input
80	GND		
81	N.C.		
82	N.C.		
83	GND		
84	TX0p	Lane 0 Tx Input I	CML Input
85	TX0n	Lane 0 Tx Input I	CML Input
86	GND		
87	TX1p	Lane 1 Tx Input I	CML Input
88	TX1n	Lane 1 Tx Input I	CML Input
89	GND		
90	N.C.		
91	N.C.		
92	GND		
93	N.C.		
94	N.C.		
95	GND		
96	TX2p	Lane 2 Tx Input I	CML Input
97	TX2n	Lane 2 Tx Input I	CML Input
98	GND		
99	TX3p	Lane 3 Tx Input I	CML Input
100	TX3n	Lane 3 Tx Input I	CML Input
101	GND		
102	N.C.		
103	N.C.		
104	GND		

# Mechanical Specifications



**About Us:**

Proline Options is one of North America's leading providers of transceivers and high speed cabling. With a reputation for quality, tested products that cover the connectivity spectrum, Proline Options has a solution for you regardless of the specification.

At Proline Options, every product is tested in its intended application - never batch or spec tested only. We run bandwidth, distance and IOS network tests. We have documented an impressive 0.03% failure rate over the last 10 years. To continue this rate of success we invest millions annually in our own on-site testing lab.



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